

## **Oscilloscope Input Overload Detection Project Closeout**

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# 1 Project timeline

## 1.1 Initial Project Development

Artifact	Due Date	Task Breakdown	Associated Meeting Time/Date, Duration and Location	Parties Involved
<b>1 Initial Project Development</b>				
1.1 Project Assignments	Week 1	<ul style="list-style-type: none"><li>• Receive assigned project</li></ul>		
1.2 Initial Project Partner Meeting	Week 2	<ul style="list-style-type: none"><li>• Meet with Brian Mantel from Tektronix</li></ul>	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams	Project Team, Brian Mantel
1.3 Project Charter	Week 7	<ul style="list-style-type: none"><li>• Revise executive summary, team communication protocols and standards, and risk register</li><li>• Create project timeline and engineering requirements summary</li><li>• Create project timeline and engineering requirements summary</li></ul>	Weekly Mon. Team Meeting, 3 - 5 pm, Discord	Project Team
1.4 Final Engineering Requirements Draft	Week 9	<ul style="list-style-type: none"><li>• Review feedback from engineering requirements draft</li><li>• Revise and confirm final requirements and testing plan</li><li>• Submit changes on student portal</li><li>• Send requirements to project partner</li></ul>	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams	Project Team, Brian Mantel
1.5 Final Block Diagram Due	Week 10	<ul style="list-style-type: none"><li>• Submit block diagram images and interface definitions through student portal</li><li>• Send copy to project partner</li></ul>	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams	Project Team, Brian Mantel

Table 1: Initial Project Development Table

## 1.2 Advanced Research and Building

Artifact	Due Date	Task Breakdown	Associated Meeting Time/Date, Duration and Location	Parties Involved
<b>2 Advanced Research and Building</b>				
2.1 Block Validations	Week 13	<ul style="list-style-type: none"> <li>Each team member completes design and validation of one block</li> </ul>	Weekly Mon. Team Meeting, 3 - 5 pm, Discord	Project Team
2.2 First Block Checkoff	Week 14	<ul style="list-style-type: none"> <li>Each team members proves that one of their blocks meets all interface properties</li> </ul>	Fri. January 15th, 3:00pm - 5:00pm, Zoom	Project Team, TA
2.3 Design Reviews	Week 15	<ul style="list-style-type: none"> <li>Sign up for slot and send project artifacts to peers</li> <li>Give presentation and review work of others</li> <li>Send commented material's to peers</li> </ul>	Thur. January 21st, 1:00pm - 3:30pm, Canvas	Project Team, Peer Reviewers
2.4 Engineering Requirements Lock	Week 15	<ul style="list-style-type: none"> <li>Engineers requirements are locked and cannot be changed after this date</li> </ul>	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams	Project Team, Brian Mantel
2.5 Second Block Check-off	Week 17	<ul style="list-style-type: none"> <li>Each team members proves that their second blocks meets all interface properties</li> </ul>	Thur. Februray 4th, 3:00pm - 6:00pm, Zoom	Project Team, TA
2.6 Submit PCB Design for Fabrication	Week 17	<ul style="list-style-type: none"> <li>Complete PCB design</li> <li>Have design review by project partner</li> <li>Submit design for manufacturing</li> </ul>	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams	Project Team, Brian Mantel

Table 2: Advanced Research and Building Table

## 1.3 Testing

Artifact	Due Date	Task Breakdown	Associated Meeting Time/Date, Duration and Location	Parties Involved
<b>3 Testing</b>				
3.1 Final Block Check-off	Week 20	<ul style="list-style-type: none"> <li>Each team members proves that their final blocks meets all interface properties</li> </ul>	Weekly Mon. Team Meeting, 3 - 5 pm, Discord	Project Team, TA
3.2 Start and Complete PCB Assembly	Week 21	<ul style="list-style-type: none"> <li>PCB should arrive during week 19 and all parts should be available for manufacturing.</li> <li>Assemble multiple copies of the PCB to begin the testing phase.</li> </ul>	Weekly Mon. Team Meeting, 3 - 5 pm, Discord	Project Team

Table 3: Testing (1 of 2) Table

Artifact	Due Date	Task Breakdown	Associated Meeting Time/Date, Duration and Location	Parties Involved
3.3 System Review 1	Week 24	<ul style="list-style-type: none"> <li>Expected to show 8 of the 12 engineering requirements functioning on the system.</li> <li>The universal engineering requirement constraints must also be met for this system review.</li> </ul>	Weekly Mon. Team Meeting, 3 - 5 pm, Discord	Project Team
3.4 Characterization Testing	Week 24	<ul style="list-style-type: none"> <li>Using equipment provided by Tektronix, complete detailed testing of PCB</li> <li>Review results with project partner</li> </ul>	Fri. May 12 pm - 5 pm, Tektronix, Beaverton	Project Team, Brian Mantel

Table 4: Testing (2 of 2) Table

## 1.4 Project Presentation

Artifact	Due Date	Task Breakdown	Associated Meeting Time/Date, Duration and Location	Parties Involved
<b>4 Project Presentation</b>				
4.1 Completed Project Close-out Packet Draft Assignment	Week 26	<ul style="list-style-type: none"> <li>Group submission of project materials and documentation.</li> <li>Project closeout packet should be completed and in the peer review process.</li> <li>Used to finalize the achievements and goals of the project.</li> </ul>	Weekly Mon. Team Meeting, 3 - 5 pm, Discord	Project Team
4.2 Project Summary Video Assignment	Week 26	<ul style="list-style-type: none"> <li>Requires a video outline before recording and the video should be 4 to 6 minutes long.</li> <li>Slides should be used to guide the video.</li> <li>Video should be recorded after having the outline and slides reviewed.</li> </ul>	Weekly Mon. Team Meeting, 3 - 5 pm, Discord	Project Team
4.3 Final System Review	Week 27	<ul style="list-style-type: none"> <li>Final verification that all engineering requirements are met</li> </ul>	Mon. May 18, 4:00pm - 5:00pm, Zoom	Project Team, TA
4.4 Project Showcase	Week 27	<ul style="list-style-type: none"> <li>Prepare quality packet of documentation that can be used to present the project.</li> </ul>	Thur. April 20 2:00pm - 3:00pm	Project Team
4.5 Complete Documentation	Week 28	<ul style="list-style-type: none"> <li>Ensure that documentation for Tektronix in format they require and up to their standards</li> </ul>	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams	Project Team, Brian Mantel

Table 5: Project Presentation Table

## 2 Scope and engineering requirements summary

The engineering requirements that we have defined below are important in creating a fully working system that is up to spec with Tektronix. This design might be employed into future oscilloscope designs so it is important

that we meet all the requirements that our project partner has specified. A few key important things is making that cost is low so it doesn't raise the cost of the oscilloscope. The design size is important so we limit ourselves to a small enough area to not take up to much PCB space. Detection speed is important to make sure that trigger within a certain period of time to protect to components of the oscilloscope from damage. Environment reliability is to make sure in various temperature's we are not falsely triggering, which is important for different locations the oscilloscope could be used in. False detection avoidance is important to make sure during normal usage we are not falsely triggering and stitching to 50 ohm impedance. Reliable detection is to make sure that when a valid overload is applied that we are able to catch at least 90% percent of them. System Output Interface Longevity is to make sure that our signal is help long enough for the processor inside the oscilloscope can detect that an overload has occurred. Then finally the voltage overload detection requirement is to make sure that we trigger for a valid overloaded signal.

## **2.1 Cost**

The system will be under \$20 (2x the current solution & excluding the attenuators) in component costs when purchased at the 1000 units quantity.

## **2.2 Design Size**

The system's components should make up no more than a total footprint area of 4 square inches (excluding the BNC connector).

## **2.3 Detection Speed**

The system will identify a signal overload within 2 seconds or less.

## **2.4 Environment Reliability**

The system will correctly detect overloads while subject to environment temperatures ranging from 0 - 50 degrees Celsius.

## **2.5 False Detection Avoidance**

The system will not identify voltages under 5.5 V as overloads.

## **2.6 Reliable Detection**

The system will detect 90% of overloads starting from room temperature.

## **2.7 System Output Interface Longevity**

The system will hold the overload output signal for at least 50 microseconds after event.

## **2.8 Voltage Overload Detection**

The system will detect an overload when the input voltage is 7 V +/- 1.4 V.

### 3 Risk register

Risk ID	Risk Description	Risk Category	Risk Probability	Risk Impact	Performance Indicator	Responsible Party	Action Plan
R1	Incompatible Interface	Technical	8%	High	Different components don't play well together	Brandon Rawson will monitor housing conditions	Reduce, plan to perform testing protocols in house to avoid weather conditions
R2	Vendor Delay	Timeline	8%	Medium	Shipping date is expected to delay the project	Bradley Heenk will keep an eye on the shipping forecast	Retain, postpone timeline or overnight parts
R3	COVID Situation Worsens	Timeline	8%	High	Access to Tektronix testing equipment and lab	Brandon Rawson check in with team members weekly	Transfer, responsible party should be changed for recovery from illness
R4	PCB Layout Issue	Technical	8%	High	Losses, noise, missing connections, and missing components causing undesired behavior	Bradley Heenk monitor PCB layout	Avoid, determine the layout issue and either fix or rework the PCB
R5	Vendor Price Change	Cost	8%	Low	Original prices increase, potentially changing out budget	Calder Wilson will monitor prices of all components on BOM	Avoid, if price of part puts system over budget, choose replacement part
R6	Testing Environment Inconsistencies	Technical	25%	Medium	Testing environment is not consistently getting correct temperature and poor data	Calder Wilson will analyze testing data to look for inconsistencies	Reduce, consult with Tektronix to change testing setup and get higher quality testing equipment

Table 6: Risk Register (1 of 2) Table

Risk ID	Risk Description	Risk Category	Risk Probability	Risk Impact	Performance Indicator	Responsible Party	Action Plan
R7	Potential for Poor Communication Between Capstone Team and Project Partner	Timeline	15%	Medium	Project Partner or capstone team is not responding to questions or request about our project in at least 5 days.	Brandon Rawson will follow up with 5 days	Reduce, be transparent with project partner and clearly establish communication protocols.
R8	Hardware Failure	Technical	20%	Medium	Circuit does not pass our specified minimum requirements	Bradley Heenk will bring spare components and equipment	Reduce, replace components that fail and have redundancy in place

Table 7: Risk Register (2 of 2) Table

### 3.1 Top Three Risks

1. First: Risk ID 6, Testing Environment Inconsistencies.

The highest risk we determined was regarding our testing environment. This risk entailed the possibility of our group not having access to valid testing equipment and or the possibility of a poor testing environment where we can't have reproducible testing conditions. This is the most important procedure of our project as this design may be used in many Tektronix oscilloscopes. Our action plan was to reduce any issues that could go wrong. This meant constructing a more elaborate testing enclosure and doing our testing in an area with ambient temperature readings.

2. Second: Risk ID 7, Poor Project Partner Communication.

The second highest risk our group decided could occur was insufficient communication with the project partner. This entails the issue where when we need either a document or information about our project and are unable to obtain them in time. We calculated this as the second highest risk from the 20% likelihood and the medium impact. We chose medium impact instead of high due to this being less important towards the end of our project compared to the begging. Our action plan involved the entire group and our strategy to mitigate this issue is by reducing the damage. We combated this by scheduling weekly meetings with the project partner so that we could always get an answer withing a week. In addition, we worked on other aspects of the project while we are either waiting or confirming various aspects from our project partner.

3. Third: Risk ID 8, Hardware Failure.

Our third highest risk was hardware failure. This would be from testing equipment to PCB component failures in our design during testing. We calculated this as our third most risk due to it being a 15 % likelihood along with a medium risk impact. Our action plan was to reduce any damage that occurs, this is regarding hardware on our PCB or testing equipment. We will kept spare components on-hand during testing in case a component fails our double check testing equipment before power up to make sure everything is connected correctly.

### 3.2 Lessons Learned and Unforeseen Risks

An important lesson learned is that a risk register table can be extremely useful to reference during times when things are going wrong. The risk register was able to point us in the right direction and assign a responsible party during certain scenarios.

One unforeseen risk was the logistics and time required to access tools that Tektronix offered us. This risk came up during times that we needed to make a commute to the Tektronix office to get access to a piece of



equipment necessary to meet our timelines. This became an issue because it was difficult to plan and decide who would make the two hour commute to the Tektronix offices.

## 4 Future Recommendations

These are recommendations that should be considered by a future team that takes of this project.

### 1. Schedule More Time for Temperature Testing

The project requires testing in the temperature controlled temperature in Tektronix's office in Beaverton to properly calibrate it. Our team scheduled only one day for testing. When the temperature is changed, the system must be left to sit for around 20 minutes to ensure that it is completely at the new temperature. This took away a lot of time from gathering data. Although we got valuable data, more time would have been desirable in order to fully prove that the system worked properly across all temperature ranges.

**Recommendation:** Schedule at least two days for temperature testing. On the first, gather performance data so that you can choose the proper resistor bias values for the temperature sensor. On the second day test the system with the chosen bias values and adjust if needed.

### 2. Change the Overload Memory Design

We noticed a slight bug with the design during simulation that if we are actively overloaded and our latch is reset. We will not latch onto another overload signal until we get another active high edge from our overloaded signal. This means the overload signal must stop and be applied again.

**Recommendation:** This can be easily fixed however by adding a single AND gate in series with the input to the latch and attaching our active low reset to the second input of the AND gate. This makes it so when we reset our latch we are also forcing an active low signal to our latch and if an overload is still present as soon as we are no longer resetting it will be captured or stay active low if the overload has disappeared.

### 3. Improve the Ramp Detection Accuracy

The ramp detection portion of the system occasionally had issues detecting rapid temperature increase overloads due to the variation in slope and temperature. This resulted in scenarios where the ramp detection would not trigger for some slopes.

**Recommendation:** Find the optimal bias values for the configuration of the ramp detection unit. Changing these values can help to detect the majority of temperature increase slopes that are most common. Another solution would be to consider a different type of design architecture for detecting rapid increases in temperature by examining the slope.

### 4. Meet With Project Partner Weekly

This project had many specifications, so it is useful to know that you are on the right track by checking in with your project partner.

**Recommendation:** As soon as project team members have their term schedules, contact your project partner and setup a weekly meeting time. Having this time to check in every week is beneficial to both the team and the project partner as it provides a regular deadline for the team to have their work done by, and provides a reminder for the project partner to complete any logistics required on the company's side.

### 5. Test the System on an Oscilloscope Front End

The previous testing was done on an isolated PCB that only contained the overload detection unit. It would be useful to test this system by adding it to the front end PCB on a Tektronix oscilloscope and ensuring that it still functions properly.

**Recommendation:** Submit this system to the proper contacts at Tektronix and have it added to the front end PCB for a prototype version of an oscilloscope that is being made for system testing. Run the system test on the oscilloscope to ensure that the overload detection system is still functioning properly.

### 6. Simulate Your Design

We didn't find out until later in the design on how important simulation is to make sure your design works and you won't have any issues. We did our project initially without any simulations and were urged by our Project Partner's to get some good simulations of the design.

**Recommendation:** Make sure to start the simulation of your design early. This will help you catch any bugs and issues you may run into in-case something doesn't work. It's also important to verify and have something to fall back and test if things go wrong.

## 7. Design System Layout To Make It Easier To Test

Our PCB had some layout issues that made testing somewhat difficult. We used jumpers to disconnect the potentiometers from the circuit so that their value could be measured. During testing, it was a tedious process to remove the jumpers between each test and reconnect the testing leads to measure. This was especially a problem when the system was in the temperature chamber. Another issue was that the power for the system and the input voltage being tested came from the same power supply, so we had to manually plug and unplug the input voltage to test it which didn't always create a clean edge. Another layout problem was too few ground test points.

**Recommendation:** Add more testpoints and use switches instead of jumpers. Also add more ground test points. In general, think of how it will be hard to access the system in the temperature chamber, so all connections need to be as simple to make as possible.

## 8. Complete Project Administrative Tasks Early

Since this project was with a real company, Tektronix, there were many administrative tasks required to get it started. We had to sign NDAs and setup Tektrnoix accounts before we were allowed to see the example circuit that our system was going to be based on. This took many weeks, so our project was slow to start. Later in the process, it took a while to figure out how to get the PCB's ordered.

**Recommendation:** Be on regular contact with the project partner early on in the project timeline to ensure that all administrative tasks are completed. This usually requires a lot of information exchange between the project partner and the group members. Send email reminders to your project partner to complete items on their end if needed, and complete your tasks on time.

## References