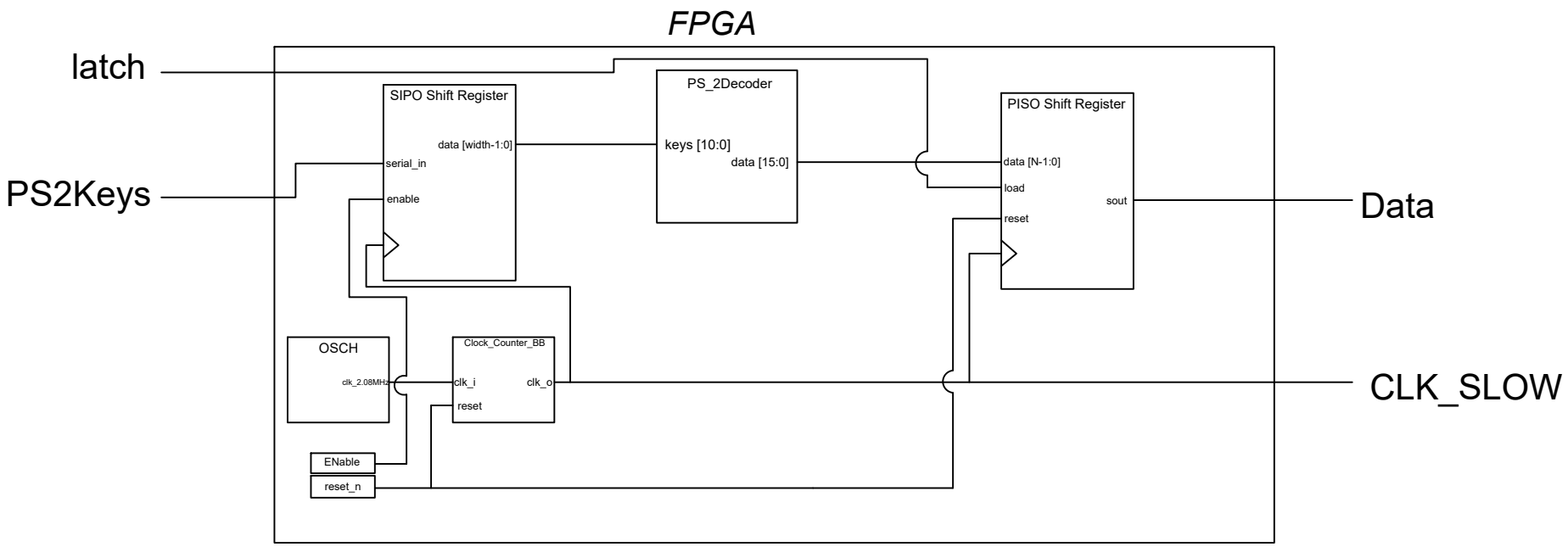
FPGA
latch
PS2Keys
SIPO Shift Register
data [width-1:0]
serial_in
enable
PS_2Decoder
keys [10:0]
data [15:0]
PISO Shift Register
data [N-1:0]
load
reset
sout
Data
OSCH
clk_2.08MHz
Clock_Counter_BB
clk_i
reset
clk_o
CLK_SLOW
ENable
reset_n