Project Closeout

ECE 443 Senior Design

Graham Mueller - Muellegr@oregonstate.edu

Benjamin Park - parkbe@oregonstate.edu

Ali Aldahish (Removed from team)

20210501

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Design Impact Statement

Public Health, Safety, and Welfare Impacts - The office is not often a physically demanding environment, yet office injuries are common and can cause long term damage[4]. Sources of this can be the sedentary nature of office jobs. A lot of investment is taken on producing ergonomic chairs that improve posture, adjustable desks, large and clear screens to reduce these injuries. These are all focused around a user at a computer for long periods of time.

One can take advantage of the investments made in more ergonomic computer setups while still being able to probe a circuit with an oscilloscope when the oscilloscope is interacted with over a computer interface.

Cultural and Social Impacts - Microscopes in schools give children the ability to see the microscopic world. Oscilloscopes let us inspect the detail on an electrical signal, something that is considered slow if it is measured in only hundreds of kilohertz. It opens the doors to them to explore and learn an entire new field, much like how microscopes can be the gateway towards life long passion that benefits society in medicine or other technologies[3].

Having more people interested in a topic brings new people into the field. This can create competition and over employment, where the previou system that could provide the needed amount of engineers is now over supplying them, reducing the future engineers leaving the system in 5-20 years in a sort of soft oscillating pattern.

Environmental Impacts - An unfortunate side effect of lower cost and reduced feature sets in electronics is a growing issue of electronic waste, or “e waste”. One website [1] cites 20-50 million tons of waste produced annually. An article by the Verge [2] provides an overall perspective, claiming a global increase in the production of electronic waste of 21% compared to 2014.

The end product of this project cycle is likely to be dispensable both because there is less of an economic incentive to preserve it and because lower cost necessitates reduced features, creating an incentive to upgrade.

Economic Factors - having the oscilloscope processing done on a computer makes it an easy task to offload this processing to servers. Servers have a large initial investment but are hyper focused towards long term return due to their low maintenance and energy costs relative to the computations needed[5]. Servers could easily solve the problem of rare but complex processing needed by each oscilloscope in a company. Instead of 100 high speed computers, it could be solved by a single high speed server and 100 low end computers.

Citations

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2. J. Calma, “Humans left behind a record amount of e-waste in 2019,” The Verge, 02-Jul-2020. [Online]. Available: https://www.theverge.com/21309776/record-amount-ewaste-2019-global-report-environment-health. [Accessed: 14-Apr-2021].
3. "Chip shortage will last beyond 2022 as demand far outstrips supply, Intel chief says" washingtonpost.com, [online] Available: https://www.washingtonpost.com/technology/2021/04/13/intel-ceo-semiconductor-chip-shortage/ [Accessed Apr 15, 2021]
4. "Office Injury Statistics" aftermath.com, [online] Available: https://www.aftermath.com/content/office-injury-statistics/ [Accessed Apr 13, 2021]
5. "Energy hogs: Servers vs. desktops vs. set-top boxes" computerworld.com, [online] Available: https://www.computerworld.com/article/2510041/energy-hogs--servers-vs--desktops-vs--set-top-boxes.html [Accessed Apr 16, 2021]

Project Timeline

Milestone	Description	Time
Project Partner Introduction	Email sent introducing the team (Graham, Benjamin, Ali) to Tektronix' project partner (Byron Farber); the purpose of the email was to establish expectations and constraints for the project	10/9/2020
Partner Zoom Meeting	Meeting with Graham, Benjamin, Ali, and Byron, to expand on the content of the introduction email	10/12/2020
Drafting of Initial Engineering Requirements	Knowing the primary constraint of the project, some possible approaches, and areas of expertise, initial requirements drafted by the whole team	10/12/2020 - 10/21/2020
Partner Review of Initial Requirements	The project partner, Byron, reviewed the initial engineering requirements for the project and gave approval	10/22/2020
Drafting of Project Charter	Expanding on the guidelines set by the requirements, the team start to outline the project components and schedule	10/22/2020 - 11/11/2020
OMBUDS Meeting	Meeting scheduled and held with the OMBUDS office to discuss the relative lack of participation from Ali	11/12/2020
Project Charter Update	Email sent to Byron linking the first draft of the project charter for review	11/12/2020
Revisions to Charter	The team continued to modify the project charter and explore the approaches expected for the project	11/12/2020 - 11/23/2020

Meetings Email	Email sent to Byron by Graham on behalf of the whole team requesting the reinstatement of regular partner meetings; Reply received with a good time for meetings	11/24/2020
December Confirmation Meeting	Graham, Ali, and Benjamin met with Byron on Zoom; relayed the contemporary state of the project and sought any advice necessary about the project trajectory/composition; Byron approved of the approach	12/1/2020
Follow-up Email	Emailed Byron as a follow-up to the 12/1 meeting; no additional questions or guidance	12/3/2020
Block 1 Development	Team independently develop their first design blocks; Graham designs front end attenuation circuits; Benjamin writes FPGA HDL code; Ali develops a power block	1/4/2021 - 1/29-2021
Winter Term Update 1	Graham sent an email on behalf of the team to update Byron on the progress of the project; Byron approved	1/28/2021
Block 2 Development	Team independently develop their second design blocks; Graham designs front end ADC; Benjamin writes Win32 GUI code for host PC software; Ali develops a power block	1/30/2021 - 2/19/2021
Winter Term Update 2	Graham sent an email to Byron updating on the project progress at the end of the term; no response from Byron	2/25/2021
Block 3 Development	Team independently develop their third design blocks; Graham designs opamp circuit; Benjamin assembles and confirms the function of a FTDI test board; Ali develops a power block	2/20/2021 - 3/11/2021

Team Change	Ali confirmed to no longer be involved in the project	4/4/2021
Final Design and Assembly of Project PCBs	Confirmation and ordering of the parts to use; finalizing front end (Graham), FPGA and USB bridge board (Benjamin); PCB drafting in CAD software; ordering of copies of the final PCBs; assembly using reflow processes and electrical testing to identify any issues	3/29/2021 - 4/20/2021
Whole System Brought Together	Front end card delivered in person in Corvallis (passed from Graham to Benjamin); Initial testing and verification of available functionality	4/21/2021 - 4/26/2021
Initial Verification	Existing functionality tested for grading purposes (Benjamin)	4/27/2021
Final Debug and Verification	Data card debugged and brought to near-full functionality (Benjamin); final verification for grading purposes	4/28/2021 - 5/17/2021

Scope and Engineering Requirements Summary

Adjustable Voltage Range	The system will measure the analog input when it exists between -3V and 10V in discernable voltage increments lower than 0.1V.
Input Bandwidth	The input bandwidth will be 10MHz or more.
Sampling Buffer	System supports a minimum of 1024 samples.
Sampling Frequency	The system will sample the input analog signal at 20MSPS or greater.
Software Control	The system will be able to receive external computer input over the same channel as the output uses. These inputs will be used to set the time scale, the voltage scale, and the triggerable voltage level.
System Output	The system will use a common wired standard to send read waveform data to a simple file on a host device (PC, oscilloscope)
Triggerable Event	The system will detect a rapidly rising edge or falling edge when the difference between 1 sample and the next exceeds 0.2v.
Variable Time Window	The system will have an adjustable time window from 2uS long to 10mS long

Risk Register

ID	Description	Category	Probability	Impact	Indicator	Person Responsible	Action Plan
T1	Circuit Layout Error	Technical	25 %	M	A presented design doesn't follow outlined needs	Individual team member	Reduce
T2	Incorrect Voltage (High/Low)	Technical	15%	L	Test voltage divider before using it on the circuit	Ali	Reduce
T3	Slow Data Throughput	Technical	10%	L	In order to get the right output we need input that execute it	Graham	Retain
T4	Error in Code	Technical	20%	H	To run the code probably	Benjamin	Reduce
T5	High Frequency Issues	Technical	30%	H	Too much power loss on traces from signal input	Graham	Avoid
T6	Failure of I/O Design	Technical	20%	M	Output hardware does not properly relay a data stream as directed	Benjamin	Avoid
T7	Component costs increase	Cost	40%	M	Increase the budget or find cheaper part's cost	Graham	Retain
T8	Power supply noisy	Technical	20%	M	Power supply generates noise in EMF range or bus voltage	Ali	Retain
T9	Github removes team tool	Timeline	10%	L	Github announces changes to tools available to free users	Benjamin	Retain
T10	Front end block falls behind track	Technical	20%	M	Team fails to develop the front end and reach milestones with its development	Individual team member	Avoid
T11	PCB insufficient for signal frequencies	Technical	20%	H	Too much power loss on traces from signal input	Graham	Avoid
T12	Failure of external interface module	Technical	20%	M	Output hardware does not properly relay a data stream as directed	Benjamin	Avoid
T13	USB interface requiring certification	Technical	10%	L	USB requires certification for use	Ali	Transfer
T14	Miscommunication	Timeline	20%	M	To clarify information in order to avoid miscommunication	Individual team member	Retain

T15	Coved-19	Timeline	50%	M	Global pandemic and if team member get sick he need to inform others	Individual team member	Reduce
T16	Part is unavailable	Logistical	30%	L	No supplier can deliver a needed part in time	Individual team member	Retain
T17	FPGA does not program	Technical	10%	H	FPGA does not respond to JTAG commands	Benjamin	Transfer
T18	Component costs increase	Cost, Technical	20%	M	Individual cost of a component increases dramatically or becomes unavailable	Individual team member	Reduce
T19	Program is not managed properly	Timeline	30%	H	Team fails to meet milestones, confusion over tasks assigned	Individual team member	Transfer
T20	Disagreements over design	Timeline, Technical	10%	H	Team diverges from a single congruent design and turns into separate competing designs with conflicting interface definitions	Team	Adjust
T21	USB fails to form a comm link with external computer	Technical	10%	L	USB and USART fails to form a connecting any external device	Ali	Transfer

The risk register was not an effective tool for the project. Having it as an assignment with too many specific metrics and wording resulted in poorly defined risks. As a result of team issues, creating a better risk assessment that was more realistic and suited to the project was simply not a priority even with the massive benefits a good risk assessment brings.

The risk register assignment is also done very early in the projects life, before all team members are oriented on the project. This compounds the issue of poorly defined risks especially when pseudo-exact numbers for likely hood are expected, but a single vague word for the action plan is expected.

A better risk register would focus on identifying risks and creating a living document that is intended to slowly be updated as the project grows and is better understood with the single largest task being to simply identify risks. The likelihood and severity blocks would be turned into 2-value systems (high/low). Setting a risk owner does not seem to do anything, so this block would be removed. The action plan would be removed and substituted with an optional description of exploration and reduction. The teams would then show that every 2 weeks, they are showing progress on reducing risks or breaking risks down into smaller separate risks as the design becomes more concrete.

An unseen issue with the risk assessment arose when many of the risks came true was resolving the issue. If the responsible party does not respond to the risk or the issue, what is the next step? When you have a team mate who does not contribute to the project but they are allowed to stay on the team, how do you enforce anything?

Future Recommendations

1. Team Leader or Manager

The team made it clear early on that there would be no leader or manager. The inability for a central authority to dictate actions was extremely detrimental to the design. If one on the team was identifying design issues and planning mistakes that required action, it would be shot down in a 2 to 1 vote.

Recommendation: Require each team have a manager that acts as a coordinator and can force team decisions on critical issues.

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2. Increase to 4 people minimum for team size for similar projects.

The work needed in this project is broad. Analog and digital signals, power handling and noise, biasing of circuits, programming across several disciplines. This touches many fields in both electrical engineering and computer science.

A team with 3 people can accomplish this project, however a minimum of two would need to have high confidence in their own abilities.

A team of 4 people allows a much tighter focus for each person on the project to learn and gain competency in.

Recommendation: Increase the team size to 4 people if selecting individuals at random.

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3. Team members that do not contribute should be swiftly removed from the team.

One of the most crippling factors, greater than even Senior Design coursework, was the surprisingly chilling effect a team member who does not need to contribute has on the team.

It was identified early on that a team member was not contributing. Responsibilities would not be completed, designs would make no sense, zero effort made towards improving.

When it came to design and planning, a lot of time would be spent re-explaining basics or asking questions towards the individual. It is also not fair for the other two team members to pick up their slack. It also creates potential issues that if the two team members design without the individual, it may appear they are excluding them.

Recommendation: Clear and outlined process to remove individuals from a team.

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4. Utilize team design resources

The team did not settle on a tool or solution towards combining group work and planning designs beyond google drive. Several ideas were proposed but these were not acted upon by the team. The inability to have a concrete design that could be easily modified and tracked was a long term and constant issue that could not be overcome.

The online senior design team portal interface is not a valid solution here. It is a slow, awkward interface that gives a poor viewpoint of the project.

Recommendation: Allow teams to track designs in their own way, in a way that is clearly communicated. There must be ways to track blocks and interfaces graphically.

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5. Create broad, medium to high risk designs to test ideas.

Senior Design course requires teams to create several prototypes that test interfaces. These were usually a waste of time, effort, and resources. Interfaces had to be awkwardly designed due to the senior design block system, made worse by the interface system.

The team could have put time and effort towards prototyping basic, low performance front ends and demonstrated FPGA programming. Things that the team identified early and repeatedly were high risk were not the focus for prototyping, leaving them high risk. **Recommendation**: Give teams freedom to choose what they will test. This would allow students to demonstrate engineering and planning, as well as working tightly with identifying risks.

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6. Increase the role of digital processing in the project

The only stated goal of the project is to produce a digital sampler at low cost. Incorporating analog elements usually associated with oscilloscopes came at a sizable cost and did not confer a substantial advantage to the performance of the system. Investigation of available components revealed digital signal processing as a commonly incorporated feature in both FPGAs and microcontrollers. It is possible that those features perform on a similar level to the first elected approach while conferring benefits in cost, reliability and versatility.

Recommendation: Investigate the use of integrated DSP components in a microcontroller or FPGA to better satisfy the main project constraint.

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7. Make use of partner resources

The first cycle of this project hasn't taken much intellectual or material input from the project's corporate partner. That introduced ambiguities in the standard for communication, collaboration, and user interfacing with the final product of the project. More regular correspondence with a contact in the partner company might confer benefits in giving a more rigorous structure to the professional aspects of the project, akin to professional practices in the company. If not required, looking to the partner for inspiration in team management might have a similar benefit. In addition, any supplemental materials the partner is willing to provide should be pursued to avoid a cost or resource constraint in the project.

Recommendation: Talk to the project partner in regular intervals not mandated by the course. Make needs known and request support. Take inspiration from their practices.

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8. Prioritize research and cost assessment early in the project cycle

Depending on the expertise of the people involved, there may be a limit to how effectively the team can draft a feasible approach to the project in a short amount of time. Even if the approach settled on is suitable given practical constraints, there may be a superior approach to the project that has been overlooked. Initial project cycle work forms the basis for the rest of the project, so ample time should be given to researching what exists in the market that applies to the project's goals. If possible, development should be deferred to the latter two academic terms of the project cycle.

The project is cost-constrained, so knowing the magnitude of financial expense for parts or tools is crucial. Assessments of cost should include leeway for possible part failures, other errors, or the need for reference boards to test designs.

Recommendation: Prioritize research early-on. Do a thorough exploration of practical approaches to the project. Do cost assessment.
