Develop Guide

- ## System overview

The overall system consists of three main parts. The first part is verifying a projection onto a VGA monitor. The verification can be as simple as displaying a color onto the monitor. The second part is the Tetris game logic. The logic takes in four different inputs. All inputs affect the location of the block. One input shifts the block right. Another input shifts the block left. The next input rotates the block clockwise. The last input rotates the block counter clockwise. The last part is the integration of the two previous parts.

- ## Electrical specifications

Monitor supply voltage
- Min: 120 volts
- Max: 240 volts

Monitor supply current
- Nominal: 0.083 amps
- Max: 0.166 amps

Operating temperature of FPGA
- Max: 150 degrees celcius

Monitor power consumption:
- 20 watt

Hsync and Vsync timing specifications:
- 25 MHz pixel clock period
- Hsync and Vsync signals run at 5v
- Horizontal timing:
    1. Front porch: 110
    2. Back porch: 220
    3. Sync width: 40
    4. Active pixels: 1280
- Vertical timing:
    1. Front porch: 5
    2. Back porch: 20
    3. Sync width: 5
    4. Active pixels: 720

- ## User guide steps

1. Collect the material in the bill of materials.
2. Research the timing specifications for the specific VGA monitor.
3. Use the quartus software to devise a project with a series of comparators to make sure the timing specification matches up the horizontal and vertical orientation output pins.
4. Verify the logic displays an image of some sort on the monitor.
5. Research how to create blocks for the tetris game in the quartus software.
6. Devise a schematic that updates the location of the blocks in the tetris game.
7. Connect the FPGA to the computer via usb port and connect FPGA to monitor via VGA port
8. Project the game logic onto the monitor.
9. Debug if there are any issues with the Tetris game logic.

- ## Design artifact figures

- Block diagram

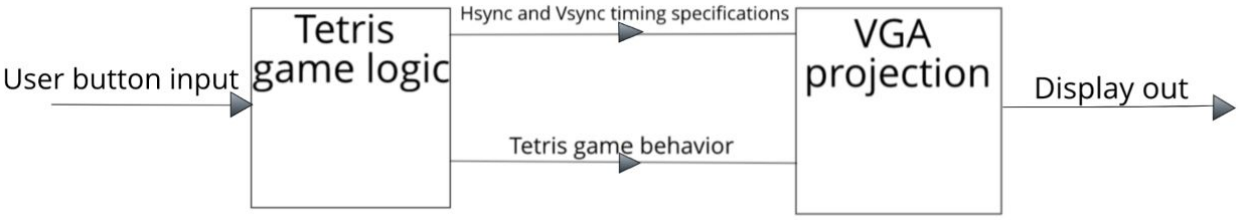

Figure 1: block diagram

The user button input into the Tetris game logic block is referring to the four buttons the user can push to affect the blocks in the following ways: shift right, shift left, rotate clockwise, rotate counterclockwise. The Hsync and Vsync timing specification input into the VGA projection block is referring to the front porch and back porch values being implemented in the system. The Tetris game behavior input into the VGA projection block is referring to the Logic of the tetris game being introduced into the system. The display out output is referring to displaying the tetris game onto the VGA monitor.

- Top level schematic

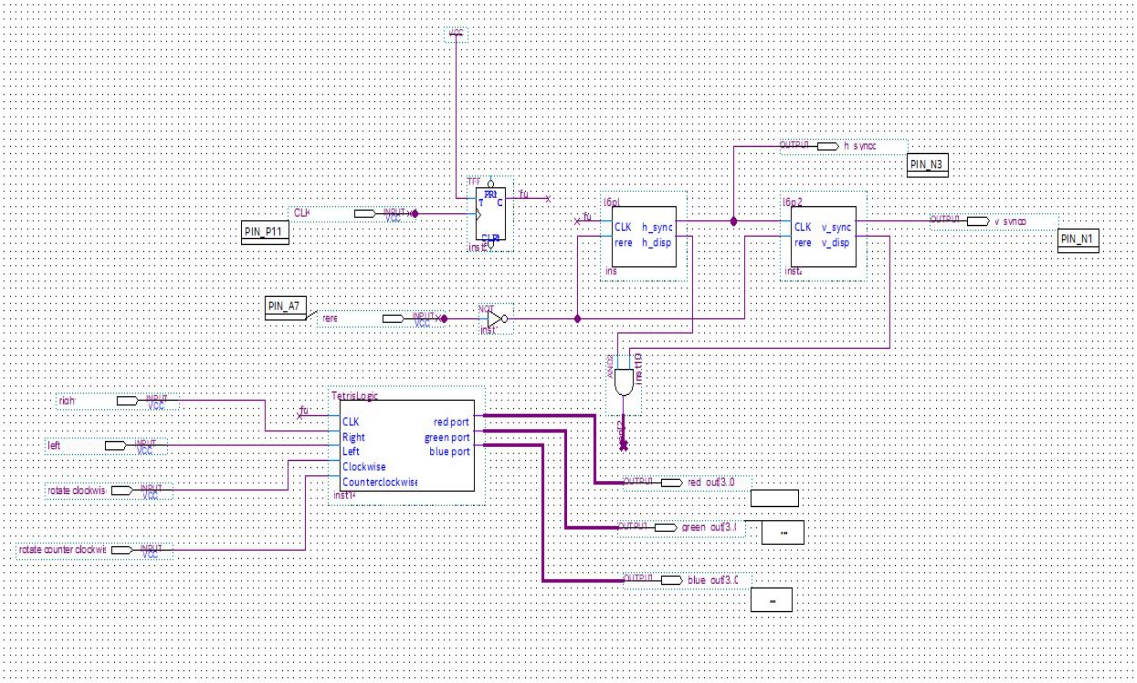

Figure 2: System top level schematic

The main components of the top level schematic are the Tetris game logic block, the H-sync logic block, and V-sync logic block. The Tetris game logic block is composed of a series of blocks. One block starts the game and the other four blocks affect the location of the tetris blocks. Both the H-sync and V-sync blocks are composed of a series of comparators to keep the timing specification in the correct range.

- Tetris game logic

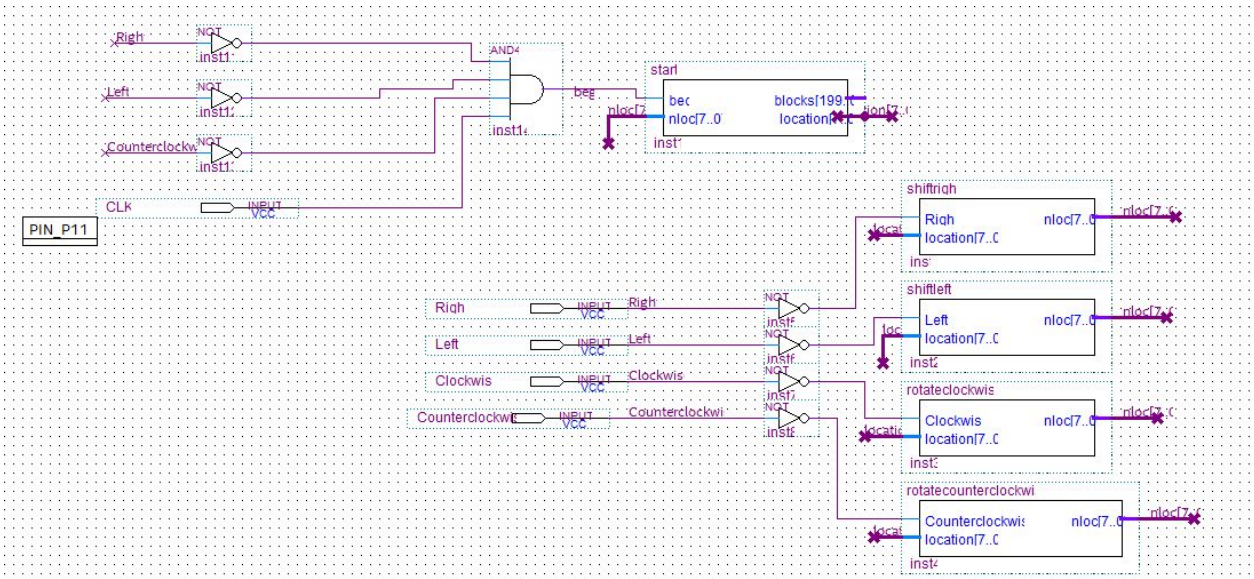

Figure 3: Tetris game logic

The Tetris game logic block is composed of a series of blocks. One block starts the game and the other four blocks affect the location of the tetris blocks which all update the current location of the current block. The first location block shifts the block to the right. The second location block shifts the clock to the left. The third location block rotates the block clockwise. The fourth location block rotates the block counter clockwise.

- H-sync logic block

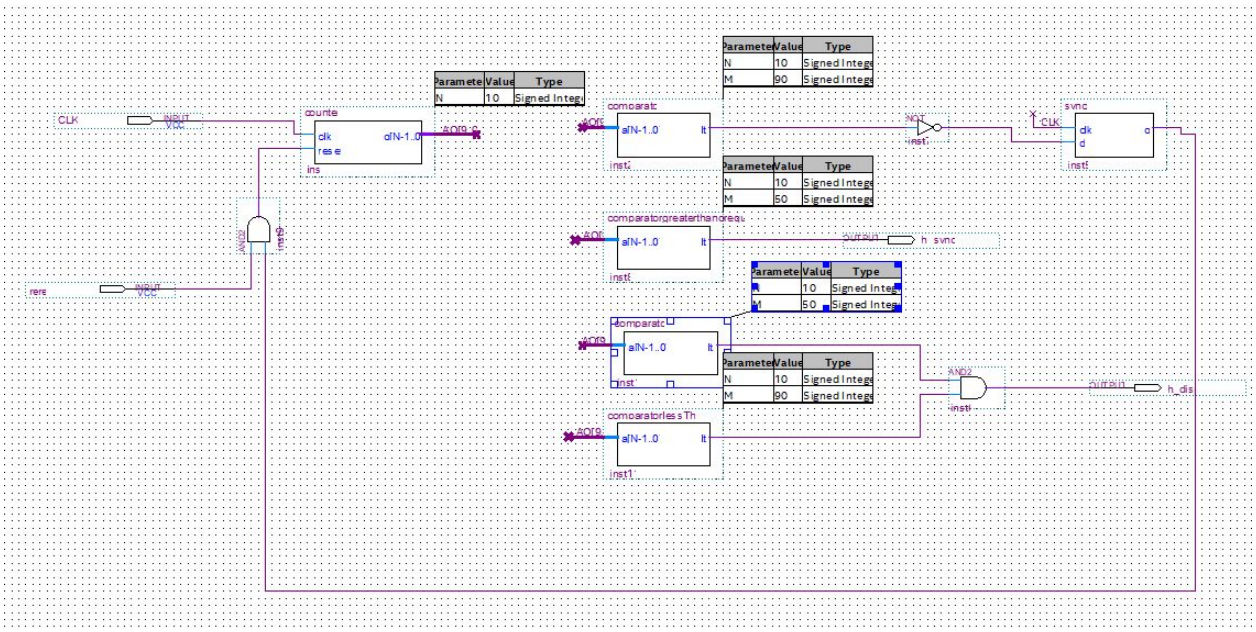

Figure 4: H-sync logic block

The H-sync block is composed of a series of comparators to keep the timing specification in the correct range. Two of the comparators are used to make sure the horizontal sync value is within specification. The other two comparators are used to make sure the horizontal display value is within specification.

- V-sync logic block

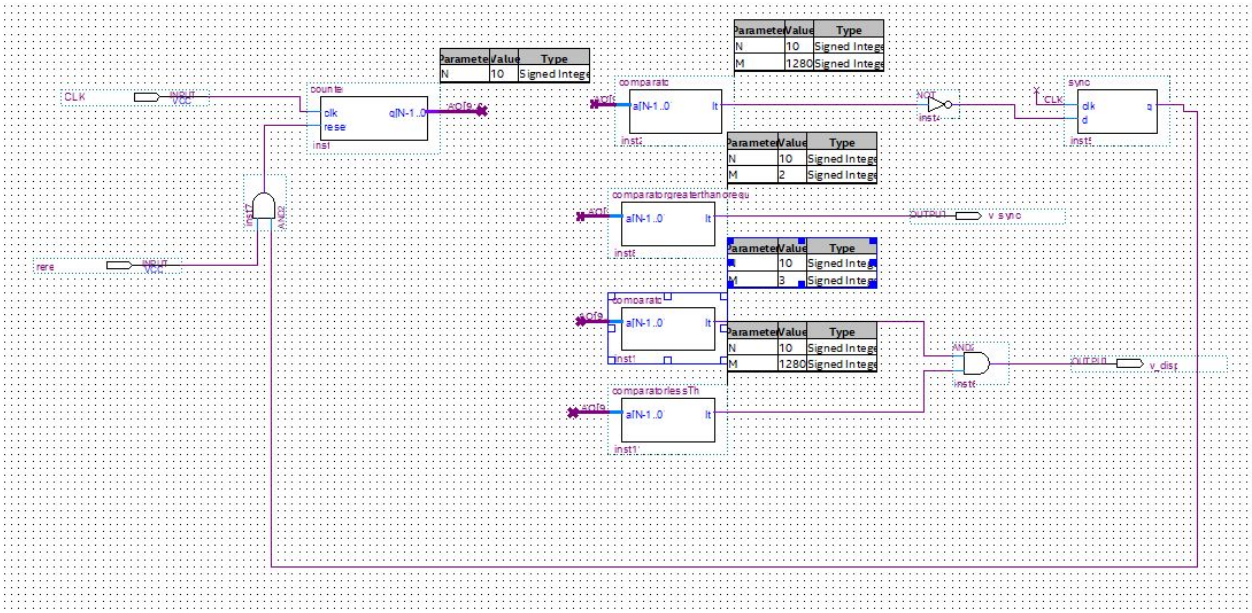

Figure 5:

The V-sync block is composed of a series of comparators to keep the timing specification in the correct range. Two of the comparators are used to make sure the vertical sync value is within specification. The other two comparators are used to make sure the vertical display value is within specification.

- **PCB information**
  - Size (LxW in millimeters): 2400x800
  - Schematic layout

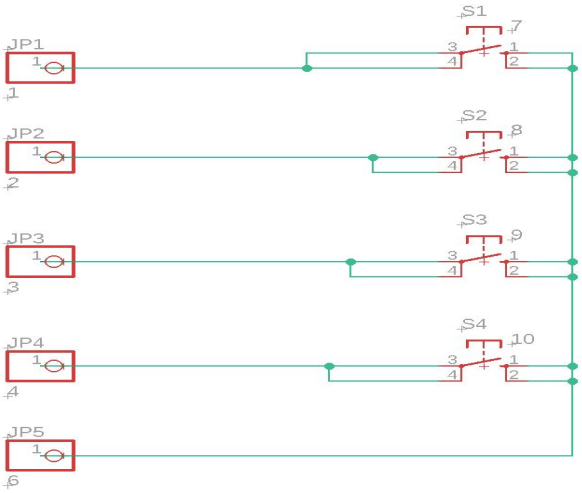

Figure 6: PCB schematic layout in Eagle

  - Block layout

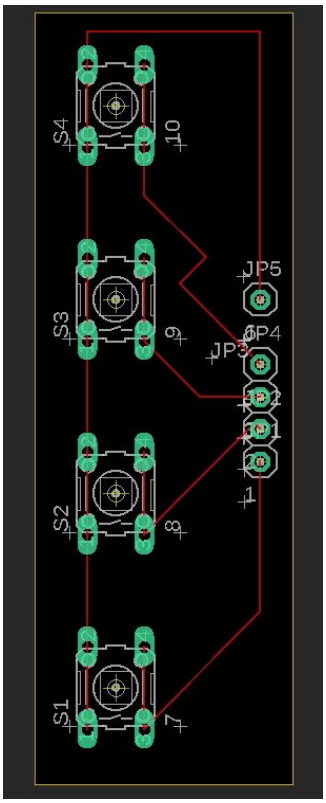

Figure 7: Block layout in Eagle

- PCB top side of finished product

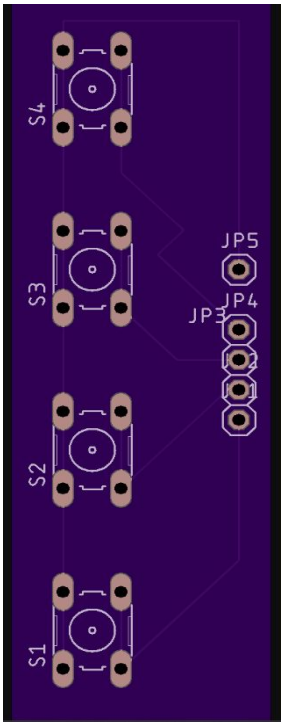

Figure 8: Top of the finished version of the PCB

- PCB bottom side of finished Product

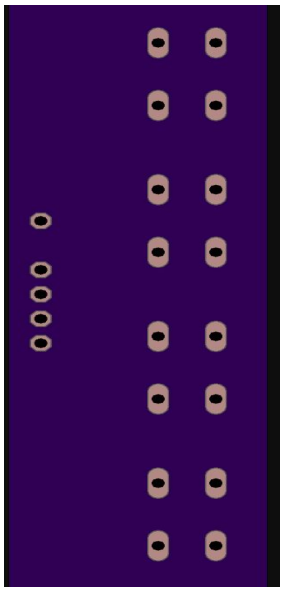

Figure 9: Bottom of the finished version of the PCB

- ## Part information

Component	Description	Quantity	Cost per unit
Monitor	1280 x 720 @ 60 Hz	1	$50.00
FPGA	Programmable microcontroller	1	$80.00
PCB board	Board used to hold button and button pins together	1	$19.10
Button	Switches to determine position of tetris shapes	4	$0.05
Solder	Uses to connect buttons to female to male header pins to terminals of switch	varies	$0.15
VGA cable	Used to project video from FPGA to monitor	1	$5.00
Female to male header pins	Used to cleanly connect the terminals of the buttons to the I/O pins of the FPGA	5	$0.77