

Project 2 - eDNA Control Board V3

Project Summary:

This project aims to redesign the current electronics board for the eDNA Project at the OPEnS Lab. From my experience using and trying to add features to the eDNA Sampler (The device that the board is for), there are some additions that I would like to make to the existing design. After negotiating with my manager, it was decided that I would add 5V sensor support, move from hardware-based sleep to software-based (microcontroller-controlled) sleep, and just general PCB layout adjustments. The problem that we were having with the current sleep system is that it does not allow for the use of external interrupts without major additions to the power circuit. The idea is to determine how much current software sleep consumes and switch to that sleep system if it fits within our power budget. The PCB layout changes mostly come from the fact that nearly none of the recommended PCB layouts are being followed when it comes to the ICs used in the current board. The final requirement that my manager selected was the creation of a document that explains the circuits and the design choices made, something that does not exist for any version of the electronics.

Engineering Requirements:

- Design and Implement a sleep circuit/mode that allows for the use of the microcontroller interrupt system and pulls no more power than the battery's passive discharge.
- The system will be able to interface with sensor inputs up to 5.5V.
- Redesign the Circuit Layout as needed and attempt to follow recommended layouts when possible. The layout will be approved by my project mentor (Don Heer).
- Documentation will be created outlining the circuit functions and design choices and approved by my boss (Chet Udell).

Testing Requirements:

- Measure the power draw from the board while in sleep mode to see if it exceeds the passive discharge of the battery.
- Use a power supply to input a 5.5V signal into the 5V sensor line and verify with an oscilloscope that it gets converted to 3.3V for the microcontroller
- The design will be approved by Don Heer (if possible)
- Documentation will be approved by Chet Udell and/or who he recommends

Project Design:

Most of the circuits on this board have already been designed and I had no intention of fundamentally changing them in this redesign. The main circuits being redesigned are the sleep circuits and the logic level converter circuit. The other circuits only get changed on the PCB Layout level, changing as many two-terminal components from 1206 to 0805 and general rearrangement of the PCB Layout.

The problem with the old sleep circuit was that to conserve power, it disabled the output of the voltage regulator. Because of this, the microcontroller was completely off, preventing conventional interrupt wake functionality. To wake up the system, the previous designer created a circuit based on a D Flip Flop where the interrupt from the RTC would trigger the D Flip Flop to enable the Voltage Regulator. This makes it difficult to add additional external interrupts to wake the system from sleep. We encountered this problem when we tried to add a button that would wake the system from sleep and trigger an operation.

The benefit of this circuit is that no components can passively consume power when not in use (when in sleep). But this type of circuit is not the only one to stop the passive consumption of unnecessary components. Another project from the OPEnS Lab created a circuit that is used by the majority of projects at the OPEnS Lab, the eDNA project being one of the projects that do not. This project called the Hypnos Board, uses a series of MOSFETs to enable and disable power lines going to peripheral devices. If every circuit except the voltage regulator and microcontroller connects to the MOSFET-controlled power lines, then the only circuit consuming power would be the voltage regulator. According to other employees at the OPEnS Lab and to online research, the OPEnS Lab microcontroller of choice, the Adafruit Feather M0, consumes 1-2mA of current while in a software sleep. Based on the size of the battery, power consumption during operation, and the size of the battery, the approximate current draw while in sleep should be little enough that the sampler can complete a full 24 operations over the course of 30 days, which is what the eDNA Sampler was designed to be able to do.

The change in the logic level converter circuit was needed because 5V I2C sensor support was desired for the eDNA Sampler. This is because many I2C sensors function off of 5V and limiting the system to only 3.3V I2C sensors can make it difficult to add desired features or functionality. The current logic level converter, a module from Sparkfun, only has 4-channels of conversion with three already in use. The second reason was that the current. Since the circuit needed to be changed anyway, instead of using a module, an IC was found to serve the purpose. The IC found was the TXS0108E.

Status at the end of the Term/406 Course:

I have met two of the four requirements, and have sort of met a third requirement. The two requirements that I have met are the 5V sensors support and the documentation requirements. I wrote up a document explaining the function of each circuit and why certain decisions were made when designing those circuits. I showed this document to one of my bosses during a meeting and they were satisfied with the result. Especially considering no documentation has ever existed explaining the function of the electronics board and why certain decisions were made.

The 5V sensor requirement was tested using a button that I could press to create a digital signal and recorded what happened on the other side of the logic level converter with a multimeter. While I did not use an oscilloscope as I had originally planned, I felt that the multimeter test was sufficient enough to test the logic level converter circuit.

The requirement that was partially met was the PCB redesign. There are some minor issues with the board, the sleep circuit is not fully tested, and I did not get the PCB verified by my project mentor. I did get the schematic and PCB looked at by a senior employee at the lab with a lot of experience and he did give the okay on what he saw. The only issues that I encountered were mistakes in connecting certain components to the MOSFET-controlled Power rails instead of the always-on power rails. The most significant component was the pull-up resistor for the RTC interrupt. Since the RTC interrupt functions by pulling the line low, when the pull-up lost power, it triggered the interrupt on the microcontroller.

What I would do differently/Future Plans:

Most of the issues that I have faced with this project and my second project this term came from poor planning and scheduling. Most of the work on all of my projects did not start until midway through the term. With three projects, I could not spend the necessary time focusing on each project in high detail. Because of this, I made mistakes, such as connecting the RTC Interrupt Pull-Up to the MOSFET-controlled power. In the future, I plan on double and triple checking any design I make a few days between each check to attempt to catch any simple errors in my designs. If possible, I will have multiple others review my designs.

I will also attempt to do what my project mentor recommended and set aside specific times to work on any projects/assignments in the future to ensure they get done in a timely manner. That will be harder to achieve but it should hopefully improve my scheduling issues and poor time management.