Plasma Speaker

ECE 441-443 - Senior Design

2021 - 2022

Kyle Barton, Ian Scott Paul, Jeffery Unrein, Zhenglun Yang

1. Overview

1.1 Executive summary

The plasma speaker project aims to develop a functional speaker by creating and controlling plasma produced by an electric arc. This technology has been demonstrated to be capable of producing speakers with excellent replication of high-frequency sound.[1][2] Plasma speakers are used in place of a solid diaphragm speaker for the tweeters in some very high-end audio systems due to the material limitations of the solid diaphragm.[1] Our system functions by creating plasma between two electrodes and modulating alternating electrical current passing through the plasma so that the ionized air responds to the produced magnetic field. The resulting movement of ionized particles interacting with the surrounding air creates sound waves. Our goal is to produce an appealing, safe, and easy-to-use plasma speaker design for display in Kelley Engineering Center.

1.2 Team Communication Protocols and Standards

1.2.1 Contact Information

Name	Phone Number	Email	Role
Kyle Barton	(360) 953-0253	bartokyl@oregonstate.edu	Digital Design
Jeffrey Unrein	(503) 910-0398	unreinj@oregonstate.edu	Power System/ Plasma Generation Design
Zhenglun Yang	(541) 740-0929	yangz5@oregonstate.edu	Software Design
Ian Scott Paul	(541) 730-2000	paulia@oregonstate.edu	Analog Design, FPGA Design

1.2.2 Partner Communication Analysis

This project is run as a general partnership of the members. To generate an ideal end-user, we collaborated to establish goals and requirements based on our preferences and understandings of the system. As such our team has no external party to communicate with, we instead have dedicated bi-weekly meeting times to discuss the project's scope and direction.

1.2.3 Communication Protocols

1. Communication with Instructors:
    a. Questions will be asked during office hours and through email

2. Primary means of Communication:
    a. Group work and communications will be conducted through Discord.
    b. Text messages will be sent for in-person updates and team building.
3. Communication Style:
    a. Group members will ensure all ideas are heard, and that all members are on the same page before making decisions.
4. External Communication Etiquette:
    a. External communication about the project will be kept professional in manner.
5. Internal Communication Etiquette:
    a. Communication towards team members will remain polite at all times.

1.2.4 Team Standards

Standard	Protocol
Meetings	- All group members will attend weekly meetings in Dearborn 211 unless otherwise agreed upon by the entire team. - All group members will be prepared for meetings and ready to participate. - Meetings will be efficient and will follow a prepared meeting outline. - Meetings will not go more than 20 minutes overtime.
Documentation	- Project documentation will be stored on the shared google drive. - All documentation and artifacts will be of professional quality. - Code will be commented on or self documenting. - All diagrams will be readable and clear.
Individual Work	- Progress on assigned tasks will be clearly communicated to the entire team. - If it is uncertain if an assigned task will be completed within the original time frame, a solution will be chosen by the team.
Team Contributions	- Work will be split up only by the decision of the entire team and each member shall be tasked with a similar amount of work.
Behavior	- Team members should always have a positive inclusive attitude. - Team members will include everyone's ideas and always provide a helping hand if needed.

1.3 Gap Analysis

1.3.1 Need Gap

Our group is providing a rarely witnessed way to listen to music/sound. This provides a more diverse and inspirational listening experience for our end users. A plasma speaker also has no resonance or transient problems, thus an improvement over conventional solid diaphragm speakers. With a plasma arc having zero weight, this creates a faster response. This makes them ideal for ultra-high-quality reproduction of high frequencies. This speaker will also be displayed in Kelley Engineering to show the capabilities of Oregon State Electrical Engineering Students. The scope of this project is to create a prototype speaker design, thus all further assessments to take the speaker into production/market the speaker will be considered only once this project is completed.

1.3.2 Project Assumptions

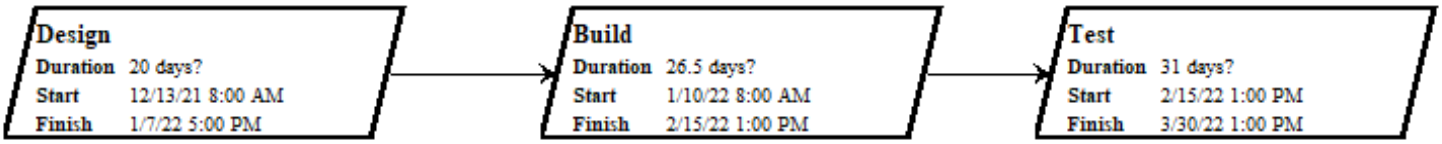
Our project assumes that it will not be capable of completely replacing a traditional audio system, and will instead be focused only on producing high-frequency audio. Our research uncovered no plasma speaker systems capable of producing low-frequency audio without significant distortion due to physical limitations in the mechanism itself. Our project also assumes that it will provide a new and exciting way to listen to music.

1.3.3 Product Expectations & Fulfillment Description

Our project will be able to produce an accurate sound from user input. The user will provide a sound using a Bluetooth connection and the system will create that sound by using the ionized air to vibrate the surrounding air. It will also have a demo button so that it can be displayed in Kelley Engineering, and when pressed play “Hail to Old OSU.” The speaker system will also have sufficient controls to change output volume and put the speaker in a standby mode. The entire system will be safe for the user and all those within the vicinity of the speaker. The entire system will be contained within a neat, user-friendly enclosure.

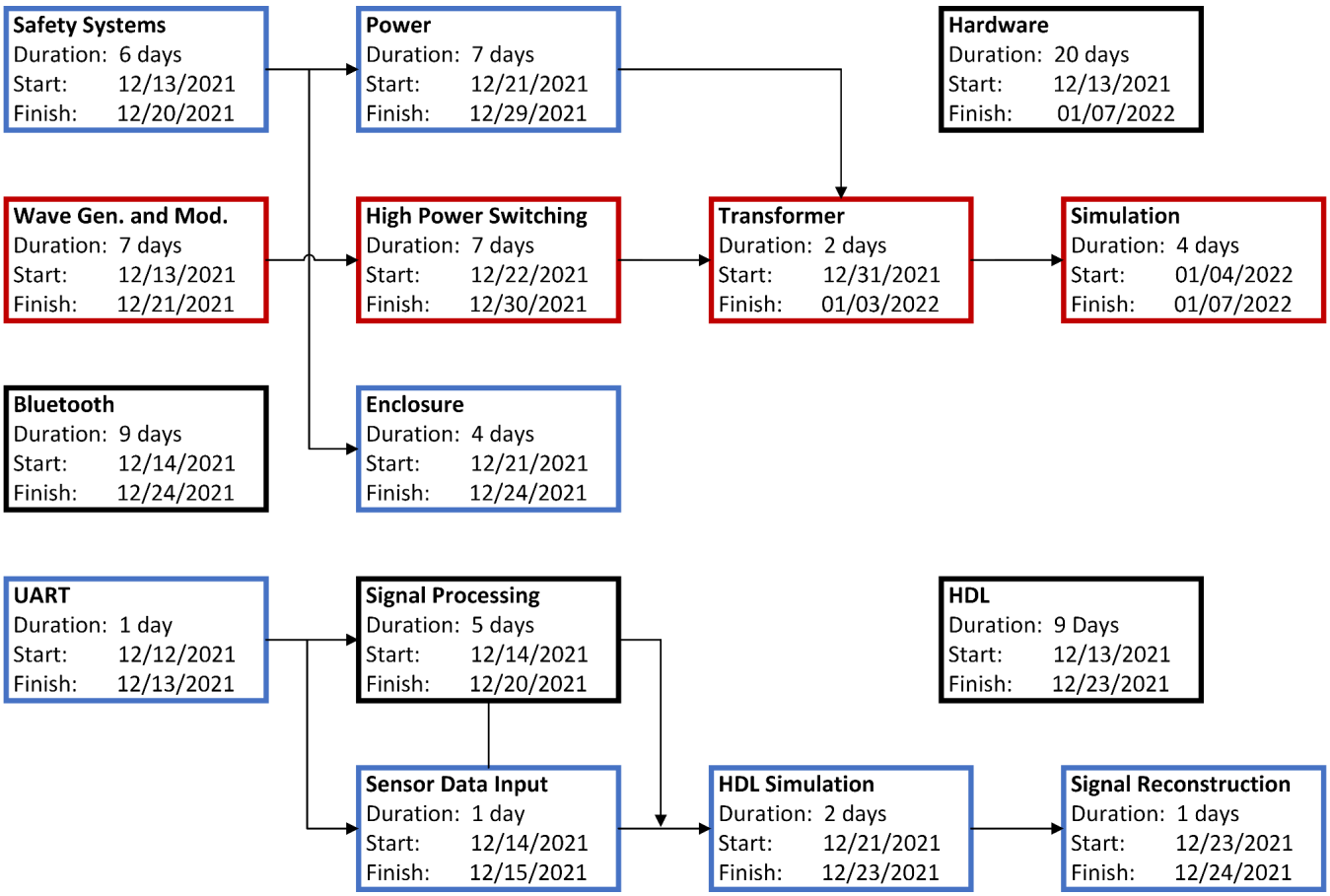
1.4 Proposed Timeline

The development of this system has been split into 3 phases: Design, Build and Test.



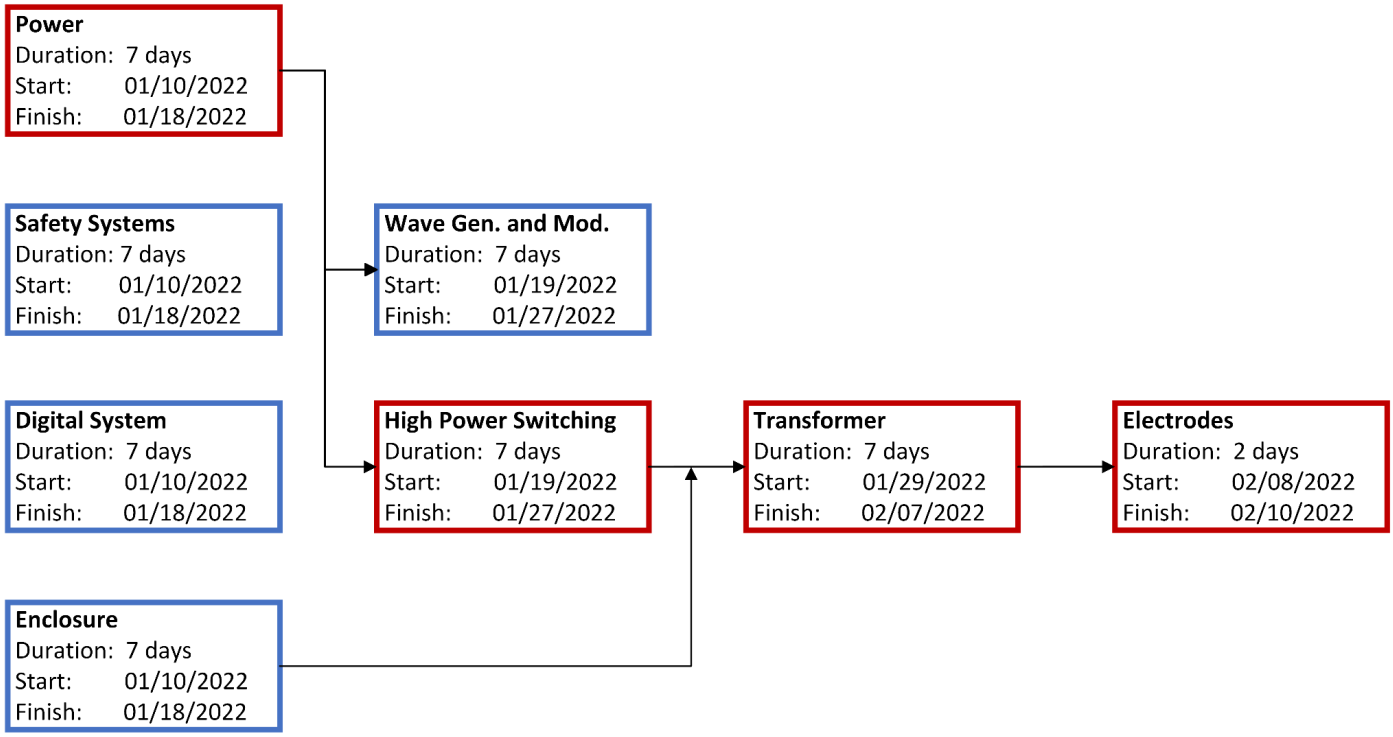
The phases of our project will be represented with a network generated from our Gantt chart in the following subsections. The full version of our Gantt chart with resource allocations is available in section 1.5.2. The critical path is highlighted in red.

1.4.1 Design



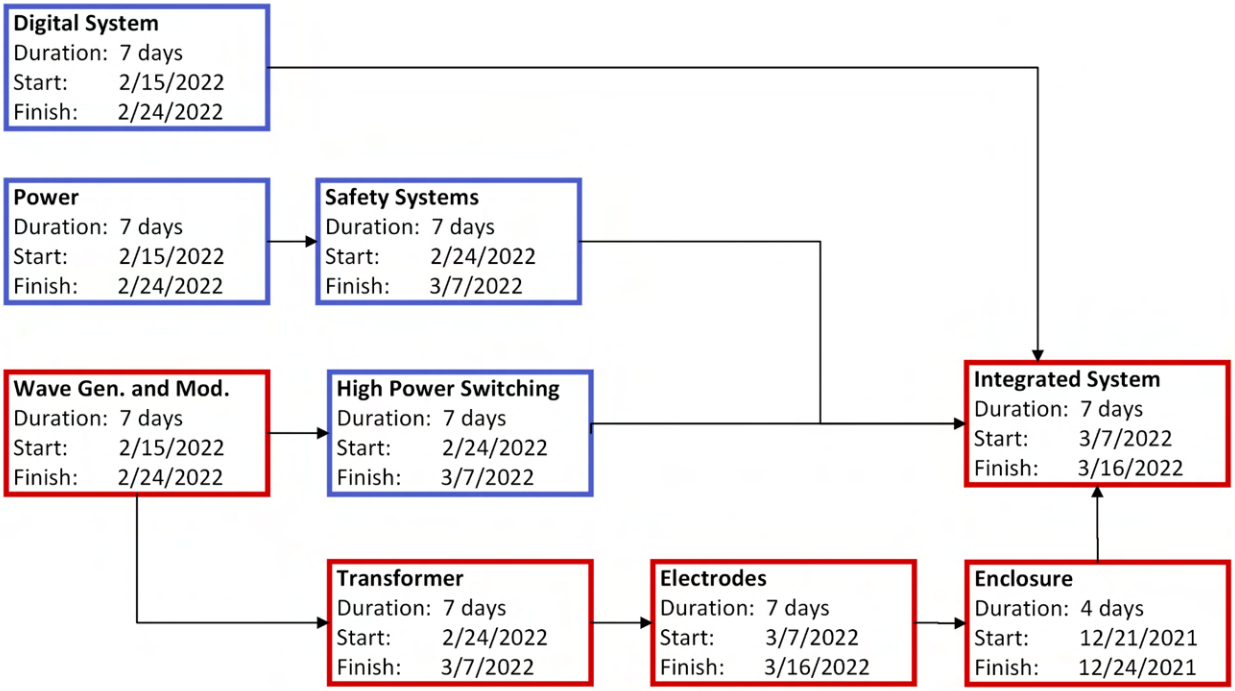
The Design phase is split into two branches: HDL and Hardware. This phase is projected to last 20 days. Our targeted deliverables are schematics and block validation writeups.

1.4.2 Build



The Build phase requires each group member to act on their design, and manufacture the physical system. This phase should result in the deliverable of several independent compatible modules ready for integration.

1.4.3 Test



The Test phase ensures individual components function as expected, and can be integrated. Each module will be added and tested sequentially to help identify any errors in integration. The test phase should deliver a fully functional plasma speaker.

1.5 References and File Links

1.5.1 References (IEEE)

[1] D. Severinsen and S. Gupta, “Design and Evaluation of Electronic Circuit for Plasma Speaker,” *Proceedings of the World Congress on Engineering*, vol. II, 2013.

[2] “Wireless/Wired Automatic Switched Plasma Tweeter & speaker ...” [Online]. Available: http://iosrjournals.org/iosr-jece/papers/Vol.%2012%20Issue%202/Version-2/D202022833.pdf. [Accessed: 13-Nov-2021].

1.5.2 File Links

Electrical Arc Speaker Team Drive - link
Project Management Guidelines - link1 - link2
Gantt Chart - link

1.6 Revision Table

Date	Topic	Revision
12/03/2021	Section 1.4	Kyle, Ian: Revised timeline to be readable
11/30/2021	Section 1.5.2	Jeffrey: Add a clickable link
11/30/2021	Section 1.1	Ian: Updated executive summary to reflect new project goal to display in KEC
11/30/2021	Section 1.2.4	Jeffrey: Formatted so text is in a table
11/30/2021	Section 1.2.2	Ian and Kyle: Updated project partner communication preferences and added model user description
11/12/2021	Section 1.5	Kyle: Updated citations to IEEE format
11/12/2021	Section 1.3	Kyle: Updated gap analysis to better describe the project expectations
11/11/2021	Sections 1.2.2, 1.2.3	Kyle: Further revision of communication protocols and team standards
11/08/2021	Section 1.4.2	Kyle: Revised project phases with more detail
11/08/2021	Sections 1.2.2, 1.2.3	Kyle: Added new communication protocols and split up team standards
11/08/2021	Section 1.4.1	Ian: Added timeline
10/29/2021	Sections 1.1, 1.3.2	Ian: Updated Executive Summary and assumptions
12/02/2021	Section 1.4	Ian and Kyle: Revised Timeline, Created Gantt chart and task network.

2. Requirements, Impacts, and Risks

2.1 Requirements

2.1.1

Project Partner Requirement: The system shall produce recognizable audio.
Engineering Requirement: Audio recognition technology “Shazam” will be able to correctly identify the source audio.
Verification method:

1. Power on the system and connect a bluetooth capable device that will play music.
2. Position another device with music recognition software “Shazam” near the enclosure.
3. Play music through the bluetooth speaker.
4. Process the audio with Shazam.
5. Verify the recognised song is the same as the source.

2.1.2

Project Partner Requirement: The system shall be responsive.
Engineering Requirement: The system begins playing audio through the arc within 2 seconds of the music being un-paused.
Verification method:

1. Power on system, connect to bluetooth, and start the flow of helium gas
2. Verify arc is not active
3. Un-pause music and verify arc is activated and playing audio within 2 second time frame

2.1.3

Project Partner Requirement: The system is safe to use.
Engineering Requirement: The system shall have an emergency shutoff switch that powers off the arc in less than 1 second.
Verification method:

1. Power system on and activate the arc by playing music
2. Using a slow motion phone video camera, place a stopwatch within frame and begin recording and begin the stopwatch
3. Also within frame and with both the stopwatch and the speaker arc on, flip the emergency shutoff switch
4. Stop recording after 3 seconds. Verify in the slow motion video that the arc was disabled within 1 second of the emergency shutoff switch being flipped

2.1.4

Project Partner Requirement: The system shall use helium gas to produce and arc.
Engineering Requirement: The system shall produce its arc in the presence of helium gas.
Verification method:

1. Power on the system and connect bluetooth.
2. Attempt to play music.
3. Verify that the system is unable to produce plasma.
4. Activate the flow of helium.
5. Verify the arc activates.

2.1.5

Project Partner Requirement: The system is contained in a safe enclosure
Engineering Requirement: The system's enclosure shall not allow users to come within 2 inches of the arc.
Verification Method:

1. Place electrodes within enclosure as they will be for final system
2. Insert measuring device through enclosure from each of the 5 sides
3. Measure from each side the distance between the environment (outside the enclosure) to the end of each electrode probe
4. Ensure that all measurements give a minimum of 2 inches from electrode probe to environment

2.1.6

Project Partner Requirement: The system must be reliable.
The system will be able to play music for 60 seconds without overheating
Verification Method:

1. Power on System and start helium flow.
2. Start input audio from connected bluetooth device
3. Use stopwatch to time system
4. Enjoy music for a minute.

2.1.7

Project Partner Requirement: The system's arc is only active when music is playing.
Engineering Requirements: System's electrical arc shall shut off within 2 seconds of the input audio signal being paused, and remain off until the audio signal is resumed.
Verification method:

1. Power system on and begin playing sound through Bluetooth audio, verify electrical arc is active
2. Pause audio
3. Verify that the electrical arc is no longer active within 2 seconds of pausing

2.1.8

Project Partner Requirement: The system is Bluetooth compatible.
Engineering Requirements: The system shall be able to play audio transmitted from a Bluetooth source
Verification method:

1. Power on the system and start helium flow.
2. Using a Bluetooth 4.0 compatible audio transmission device, investigate the Bluetooth connection menu.
    a. This will be different depending on the outside device used.
    b. The outside device must have its bluetooth mode active, and be set to "scan" or "search" for new devices.
3. Locate a device called "BT5.0 Audio"
4. Attempt to connect to the device via Bluetooth
5. Verify the connection is made and the system is recognized as an audio output.
6. Play some audio at full volume.
7. Verify arc speaker activates.

2.2 Design Impact Statement

This section presents a brief overview of the impacts of our design for readability.
A detailed analysis of the impacts is available here: Full Design Impact Assessment.

2.2.1 Public Health: Avoiding Ozone & Preventing Burns

Due to the high risk of electric shock and burns associated with voltages high enough to break down air, the safety of the designers and end users of the system is a priority.

Following our risk assessments our team opted to use helium gas as it is easier to ionize, allowing for a lower voltage to create an electric arc. Since the typical composition of air is mostly Nitrogen and Oxygen gas ($\mathbf{N_2}$ and $\mathbf{O_2}$), its ionization ultimately allows for the formation of Nitrous Oxide ($\mathbf{N_2O}$), Nitric Oxide (**NO**), and Ozone($\mathbf{O_3}$)[1]. The use of helium stops the formation of these gasses by forming the arc in an area saturated with the monatomic gas.

Due to the lightest noble gas only having two protons, it's relatively easy to ionize. The significantly lower voltage required reduces both the risk of electric shock and the risk of thermal burns from touching overheated components within the system.

2.2.2 Welfare Impacts

One potential welfare impact to consider is the dangers of loud noise. Although this is a smaller source of risk within the scope of our project, it is still important to examine. Our electrical arc speaker will be designed to operate at safe loudness levels, but malfunctions in the system could cause unpredicted loud noises. Electrical failures at high voltage often produce sudden 'popping' noises that are short term bursts which can be in the excess of 130+ decibels. Yale University School of Medicine research shows that a single burst of 140 dB can cause long term effects and lead to hearing loss [2].

2.2.3 Culture and Society: Animal Testing and Cultural Impacts

We did not end up performing animal testing, but the center frequency for our system is just above the range of humal hearing but within the range of many other animals[3]. Simply said, as of right now running our system is like blowing into a dog whistle.

Due to the high cost and appant safety considerations, it is unlikely that this will become a common consumer replacement of current speaker systems. That said, they can still be a useful educational and inspirational tool given the wide impact of music.

2.2.4 Environmental Considerations: No Light Matter.

One well documented environmental impact of electronics is the known problem of E-waste. Every electronic device has a limited lifespan and will need to be disposed of at some point. A study by Brett Robinson showed that the elements that make up the most harmful

environmental contaminants are “Pb, Sb, Hg, Cd, Ni, polybrominated diphenyl ethers (PBDEs), and polychlorinated biphenyls (PCBs) [4].” Analyzing our system, it is likely that the end product will only contain one or two of these targeted high impact pollutants; polychlorinated biphenyls and possibly lead. To mitigate this risk and be thoughtful of the eventual disposal of the electrical arc speaker, one option is to consider RoHS compliant lead-free components and manufacturing. This manufacturing technique is popular for the European market due to stricter environmental regulations. The benefit of it being fairly widely used is that there is infrastructure set up already to create a design to be RoHS lead-free. Many chip manufacturers create and sell lead-free versions of their chips at only a marginally higher price. The biggest sacrifice to going lead-free is the manufacturing and assembling of your PCBs as it limits your package and solder styles. For example, large tight pitch BGAs are often difficult and expensive to implement lead-free as the reduced flow of the lead-free solder makes them harder to align and more prone to cracking.

Along with this, the choice to use Helium is double-sided. Helium is a noble gas, and is lighter than the majority of the atmosphere. This means that it won’t bind to anything and instead will escape the planet by moving to the very outer edge of space. It is a particularly important element to conserve until its production in nuclear fission facilities is made into a reality. Currently the only helium accessible to us is a byproduct of natural gas extraction, where it is still produced by radioactive decay. [1]

2.2.5 Economic Factors

The major economic impacts of the electrical arc speaker will likely fall on the design team. The worldwide Covid-19 pandemic has had a major impact on all areas of the electronics market. A recent study from IEEE that investigates this impact and found that there is an increased need in the consumer electronics market, along with a decreased supply in the consumer electronics market [5]. Basic supply and demand tells us that these two factors cause severe price increases. If our speaker is cheap, easy to manufacture, and easy to source the materials for, we can make an impact on this squeezed market and help equalize the economic factors back to a normal level.

The other more direct impact that the Covid-19 pandemic will have on our project is the current state of the semiconductor and IC market. A study by the Federal Reserve Bank of Cleveland analyzes the behind the scenes of the current microchip shortage that likely everyone is now aware of. The study finds that the weak points in the supply chain for microchips collapsed when Covid hit, and thus a shortage arose [6]. The current lead time on specialized ICs is very commonly 52+ weeks or even listed as out of production.

Given it’s primary public use as filling balloons, the only local sourcing possible was through a party supply store where we were charged $50 per tank.

2.3 Risk Assessment

Risk ID	Risk description	Category	Probably	Impact	Performance indicator	Responsible party	Action plan
1	Member sick	Team	M	L	Team member not able to join team meetings due to a sickness	Jeffrey U.	Retain
2	Member injured	Team	L	H	Team member not able to get required work done due to external injury	Kyle Barton	Retain
3	Chip shortage delays	Timeline /Cost	M	M	Lead times on Chips are more than 2 months	Ian Scott Paul	Reduce by ordering early and extra
4	Part of the project did not work (Power, code, etc…)	Team	M	H	A team member should help each other to figure out the problem	Yang	Retain
5	Team communication issues	Team	L	H	Not everyone responding or participating in group chats/ meetings	Kyle Barton	Reduce by mediation
6	PCB long lead times	Team	M	M	Lead times on PCBs are more than 2 months	Kyle Barton	Reduce by planning ahead

2.4 References and File Links

2.4.1 References (IEEE)

[1] Kroschwitz, Jacqueline I., executive editor, and Mary Howe-Grant, editor. Encyclopedia of Chemical Technology, 4th edition. John Wiley and Sons, Inc., 1993.

[2] Rabinowitz, P.M. “Noise-Induced Hearing Loss,” Yale University School of Medicine, New Haven, Connecticut. American Family Physician, no. 61, p. 2749-2756, Oct 2000.

[3] Purves D, Augustine GJ, Fitzpatrick D, et al., editors. Neuroscience. 2nd edition. Sunderland (MA): Sinauer Associates; 2001. The Audible Spectrum. Accessed on: Dec. 2, 2021. Available: https://www.ncbi.nlm.nih.gov/books/NBK10924/

[4] B. H. Robinson, “E-waste: An assessment of global production and environmental impacts,” Science of The Total Environment, vol. 408, no. 2, pp. 183–191, 2009.

[5] T. Coughlin, “Impact of covid-19 on the Consumer Electronics Market,” IEEE Consumer Electronics Magazine, vol. 10, no. 1, pp. 58–59, 2021.

[6] J. E. Dunn, “Covid-19 and Supply Chains: A year of evolving disruption,” Cleveland Fed District Data Briefs, 2021.

2.4.2 File Links

Complete risk register with progress updates - link

Complete engineering requirements with progress updates - link

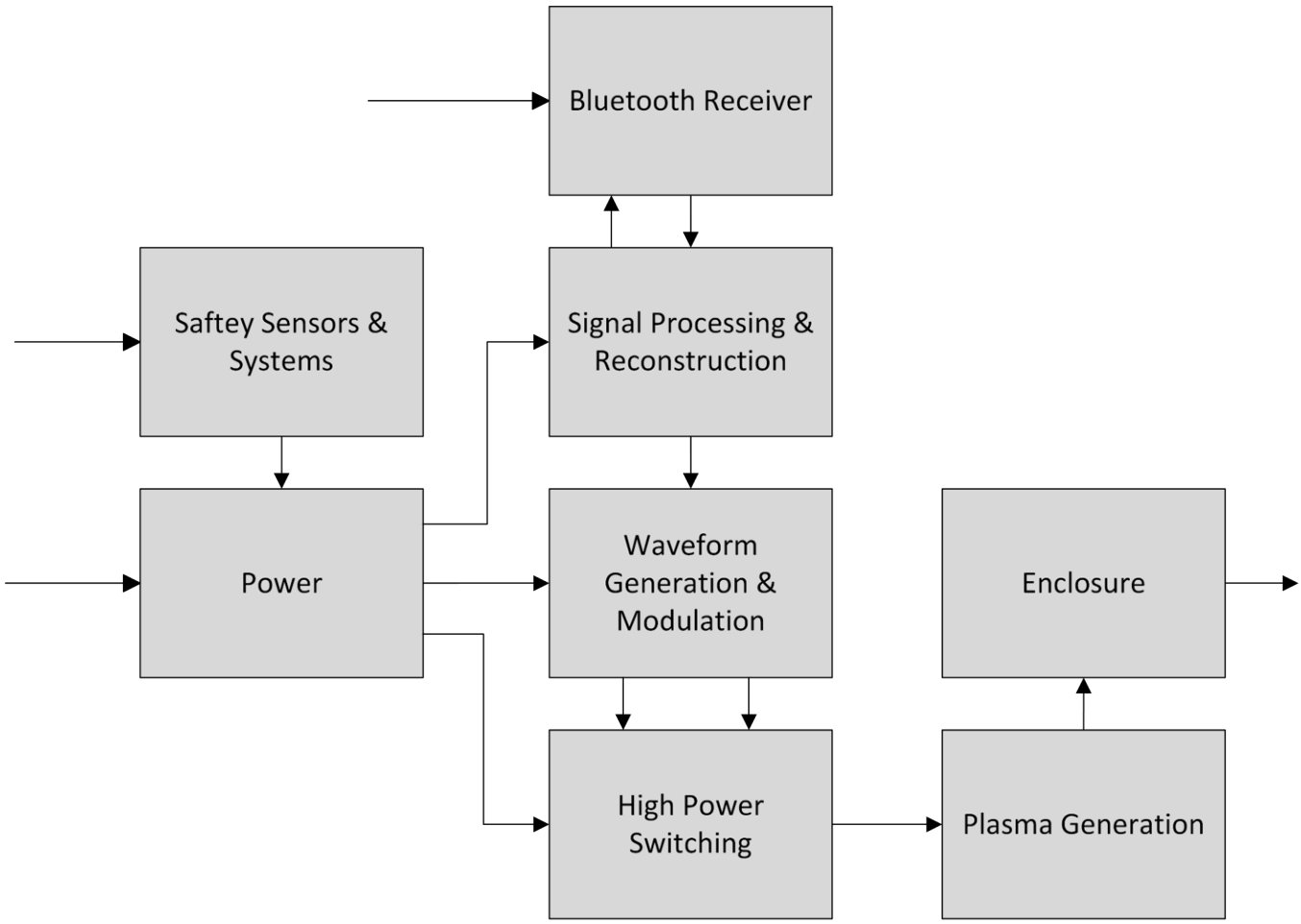
2.5 Revision Table

Date	Topic	Revision
05/06/2022	Section 2.2	Ian and Kyle: Added DIA and updated citations
03/06/2022	Requirement 2.1.5	Kyle: Updated requirement 2.1.5 verification method
11/30/2021	Section 2.1	Team: Fully reworked requirements and verification methods

11/30/2021	Section 2.4	Jeffrey: Separated into two different subsections
11/11/2021	Not enough requirements Some Requirements are not measurable	Team: Reworded some of the requirements. Added additional requirements.
11/11/2021	Performance Indicator not filled out	Jeffrey: Filled out performance indicator for all risk
11/30/2021	Section 2.3	Yang: Update new risks

3. Top-Level Architecture

3.1 Block Diagram



3.2 Block Descriptions

3.2.1 Safety, Sensors, & Systems

Block Champion: Ian Scott Paul

This block is to ensure our system is safe to use for ourselves and users other than ourselves. Our team's safety system will have an emergency cutoff switch for an outside user to press at any time of the system's operation. This block will be directly connected to the power block so that the main power can be shut off at any point. This block will also be responsible for monitoring the system’s sensors and delivering digital control to all necessary components. This block will also be responsible for triggering fault signals based on sensor data. Another function of the Safety system is to put the speaker into an ‘idle mode’ when no audio input is detected by the Bluetooth receiver block. All of this functionality will be implemented on the system’s FPGA.

3.2.2 Power

Block Champion: Jeffery Unrein

This block will be used to power the entire Electric Arc system. This block will take in 120 VAC from a wall plug-in and output two different DC voltages. One of these voltages will power the FPGA board that powers the BlueTooth, PWM, and safety sensor blocks. The other voltage will power the high power switching and plasma generation blocks. These two separate voltages will ensure that each component in those blocks is receiving the right amount of power.

3.2.3 Enclosure

Block Champion: Kyle Barton

This block is the physical enclosure for the entire electrical arc speaker system. This includes the mounting and layout of all the various subsystems in a well-thought-out and efficient manner. This block will also facilitate the speaker system's ability to connect to the end-user. This enclosure will be aesthetically pleasing and mimic a professional/commercial level design. This enclosure will also be designed so that the system is safe to the end-user, preventing any contact or proximity to the high voltage signals. Other aspects of this block include good acoustic properties and an intuitive and easily accessible button to play the speaker’s demo song.

3.2.4 Bluetooth Receiver

Block Champion: Zhenglun Yang

The Bluetooth Receiver block will wirelessly receive user input and digital music data from outside the system and deliver them to the Signal Processing and Reconstruction block. This enables the system to receive the music data digitally, so no sampling has to be done before signal processing can occur. The Bluetooth receiver also adds a layer of safety by enabling the user to interact with the system remotely. The system will show up to other Bluetooth devices as “Plasma Speaker”, and will be flagged for them as an audio output device.

3.2.5 Signal Processing and Reconstruction

Block Champion: Ian Scott Paul

As plasma speakers typically have significant distortion due to the movement of the arc and displacement of the air, it is necessary to perform signal processing on the input audio to counter the effects caused by the rest of the system. By creating a parameterizable finite impulse response filter in Matlab and implementing it on an FPGA, real-time signal processing of the streamed digital audio data is achieved. Much of the fine-tuning will require the entire system to be implemented in order to calculate the actual frequency response.

3.2.6 Waveform Generation and Modulation

Block Champion: Zhenglun Yang

Taking the analog audio signal as an input, the WGM block will modify the duty cycle of a square wave. This modulation is what implants the audio within the eventual high power signal. The modulated square wave is then split into a buffer and an inverter to create mirrored signals perfectly in phase. This is used to create the push-pull characteristics needed to sustain high voltage. This will be implemented with 3 different integrated circuits, one for pulse width modulation, one buffer, and one inverter.

3.2.7 High Power Switching

Block Champion: Kyle Barton

Since the integrated circuits in the Waveform Generation and Modulation block are not capable of providing enough power to the Plasma Generation block, the waveforms are instead used to drive high power FETs. These will be large transistors with heatsinks.

3.2.8 Plasma Generation

Block Champion: Jeffrey Unrein

The Plasma Generation block consists of the transformer and electrodes used to amplify the voltage to create the electric arc. This is used to step up the voltage nearly 800 times for the electrodes. This block may also include large capacitors to speed up the circuit's transient response and provide instant voltage to the electrodes for the high-frequency sound signals.

3.3 Interface Definitions

Name	Properties
otsd_pwr_acpwr	• **Inominal:** 15 Amps • **Other:** 60 Hz • **Vnominal:** 120 Volts
otsd_sfty_snsrs_envin	• **Temperature (Absolute):** 100 Celsius (IR temp) • **Temperature (Absolute):** 100 Celsius (Air/sensor temp) • **Water:** No water. 0CFS, no immersion.
otsd_bltth_rcvr__rf	• **Other:** Vmin: 0V Vmax: 5V Imin: 0 mA Imax: 10 mA • **Protocol:** WAV/MP3 • **Protocol:** Bluetooth 4.0 A2DP
pwr_hgh_pwr_swtchng__dcpwr	• **Inominal:** 1A • **Ipeak:** 5A • **Vmax:** 40V • **Vmin:** 24V
pwr_plsm_gnrtn_dcpwr	• **Inominal:** 3 Amps • **Ipeak:** 4.5 Amps • **Vmax:** 20 Volts • **Vmin:** 10.5 Volts

pwr_sgnl_prcssng_rcnstrctn__dcpwr	• **Inominal:** 150milliAmps • **Ipeak:** 500 milliAmps • **Vmax:** 5.5 Volts • **Vnominal:** 5 Volts
pwr_wvfrm_gnrtn_mdltn_dcpwr	• **Inominal:** 0.004 Amp • **Ipeak:** 0.100 Amps • **Vmax:** 11 Volts • **Vmin:** 5 Volts
hgh_pwr_swtchng__plsm_gnrtn_acpwr	• **Inominal:** 1A • **Vmax:** 40 VAC • **Vmin:** 24 VAC
sgnl_prcssng_rcnstrctn__wvfrm_gnrtn_mdltn_asig	• **Max Frequency:** 20K Hz • **Vmax:** 1.5V • **Vrange:** +-1V
sgnl_prcssng_rcnstrctn__bltth_rcvr__dcpwr	• **Inominal:** 5m A • **Vmax:** 5 V
sfty_snsrs_pwr_asig	• **Other:** Active High • **Vmax:** 3.5 Volts • **Vrange:** 0 - 3.5 Volts
wvfrm_gnrtn_mdltn_hgh_pwr_swtchng__asig	• **Max Frequency:** 25K Hz • **Other:** Logic Level: 10V
bltth_rcvr__sgnl_prcssng_rcnstrctn__dcpwr	• **Other:** Vrange: +-1V • **Other:** Max Frequency: 20K Hz • **Vmax:** 1.5V

3.4 Reference and File links

3.4.1 References (IEEE)

3.4.2 File Links

Student Portal - link

3.5 Revision Table

Date	Topic	Revision
5/1/2022	Interface Definitions	Team: Complete Interface definitions in the student portal and insert table.
12/1/2021	Interface Definitions	Team: Complete Interface definitions in the student portal and insert table.
11/30/2021	Block Diagram	Kyle: Reformatted block diagram with larger text and easier to read colors
11/22/2021	Block Descriptions	Team: Wrote block descriptions of our blocks
11/22/2021	Block Diagram	Team: Updated block diagram to an 8 block format from the original 12 blocks

4. Block Validations

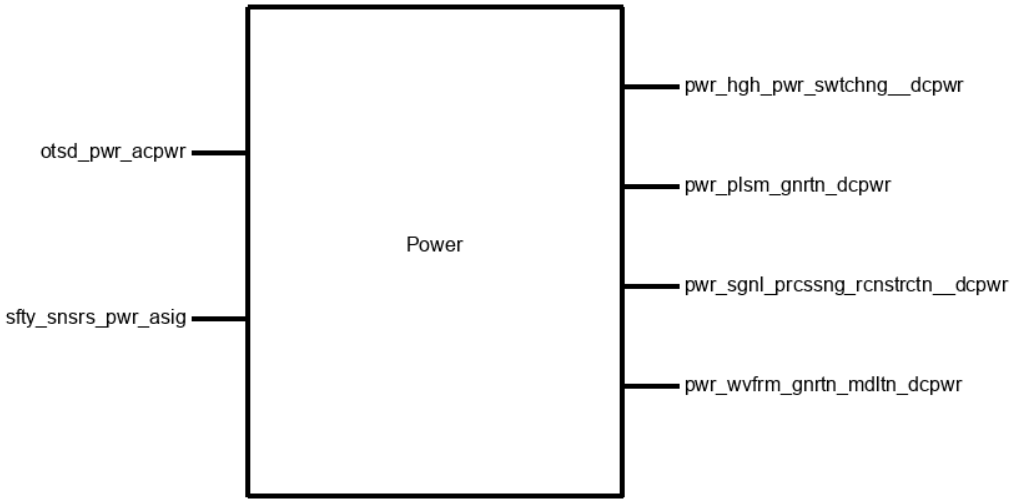
4.1 Power Block

4.1.1 Description

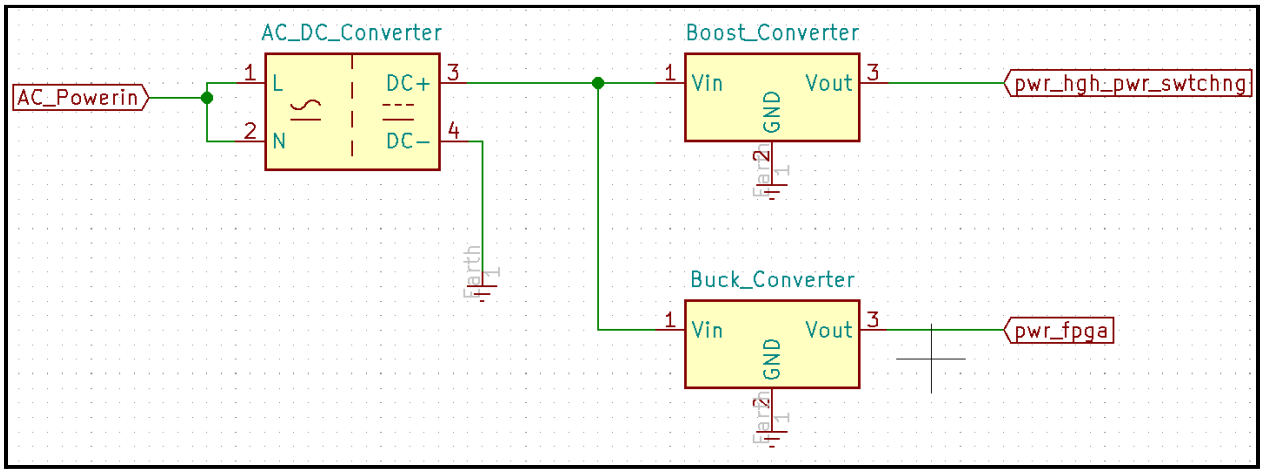
This block will be used to power the entire Electric Arc system. This block will take in 120 VAC from a wall plug-in and output two different DC voltages. One of these voltages will power the FPGA board that powers the bluetooth, PWM, and safety sensor blocks. The other voltage will power the high power switching and plasma generation blocks. These two separate voltages will ensure that each component in those blocks are receiving the right amount of power.

4.1.2 Design

Black Box Diagram:



Schematic:



4.1.3 General Validation

This block will utilize an AC - DC converter to convert AC power from a wall plug in and provide a steady DC output. It will then use 2 voltage regulators in parallel to supply two separate voltages to our system. By using voltage regulators instead of dropping down the voltage with resistors I will be able to ensure the correct amount of voltage is going to each of our components.

4.1.4 Interface Validation

Interface Property	Why is this interface this value?	Why do you know that your design details <u>for this block</u> above meet or exceed each property?
otsd_pwr_acpwr : Input		
Inominal: 15 Amps	Current is based on how much the breaker can handle. This is the average amount of current we plan on drawing.	The AC to DC converter max input current is rated to 15 Amps [1]
Other: 60 Hz	This is the frequency AC power switches at in the U.S	The AC to DC converter max input frequency is rated to 63 Hz [1]
Vnominal: 120 Volts	This is the average voltage in a wall socket in the U.S	The AC to DC converter voltage minimum is 110 Volts and its

		maximum is 220 Volts [1]

pwr_plsm_gnrtn_dcpwr : Output

Inominal: 3 Amps	This is the average amount of current being drawn when arc was established	Voltage regulators tend to need the same input current as they do output. The AC-DC converter is able to produce a current of 40 Amps [1]
Ipeak: 4.5 Amps	This is the peak current that was drawn when creating the arc	Voltage regulators tend to need the same input current as they do output. The AC-DC converter is able to produce a current of 40 Amps [1]
Vmax: 20 Volts	This is the maximum voltage needed to produce the arc	I will use the Shenghao SH-PWS3 voltage regulator which has a varying output voltage to satisfy both the max and minimum voltages needed to produce the arc.
Vmin: 10.5 Volts	This is the minimum voltage needed to produce the arc	I will use the Shenghao SH-PWS3 voltage regulator which has a varying output voltage to satisfy both the max and minimum voltages needed to produce the arc.

pwr_sgnl_prcssng_rcnstrctn__dcpwr : Output

Inominal: 150milliAmps	This is the nominal current used by the components in this block as tested by one of my groupmates	Voltage regulators tend to need the same input current as they do output. The AC-DC converter is able to produce a current of 40 Amps [1]
Ipeak: 500 milliAmps	This is the peak current used by the components in this block as tested by one of my groupmates	Voltage regulators tend to need the same input current as they do output. The AC-DC converter is able to produce a current of 40 Amps [1]
Vmax: 5 Volts	This is the maximum voltage	I will use a LM2596 voltage

	needed to ensure components are provided enough power to work. This was tested by one of my groupmates	regulator that has a varying output voltage to satisfy both the max and minimum voltages needed by this component
Vmin: 4.5 Volts	This is the minimum voltage needed to ensure components are provided enough power to work. This was tested by one of my groupmates	I will use a LM2596 voltage regulator that has a varying output voltage to satisfy both the max and minimum voltages needed by this component

pwr_wvfrm_gnrtn_mdltn_dcpwr : Output

Inominal: 0.004 Amp	This is the nominal current used by the components in this block as tested by one of my groupmates	Voltage regulators tend to need the same input current as they do output. The AC-DC converter is able to produce a current of 40 Amps [1]
Ipeak: 0.1 Amps	This is the peak current used by the components in this block as tested by one of my groupmates	Voltage regulators tend to need the same input current as they do output. The AC-DC converter is able to produce a current of 40 Amps [1]
Vmax: 11 Volts	This is the maximum voltage needed to ensure components are provided with enough power to work. This was tested by one of my groupmates	I will use a LM2596 voltage regulator that has a varying output voltage to satisfy both the max and minimum voltages needed by this component
Vmin: 5 Volts	This is the minimum voltage needed to ensure components are provided with enough power to work. This was tested by one of my groupmates	I will use a LM2596 voltage regulator that has a varying output voltage to satisfy both the max and minimum voltages needed by this component

sfty_snsrs_systms_pwr_asig : Input

Vmax: 3.5 Volts	This is the maximum voltage that could be sent to switch.	I will be using the SRD-12VDC-SL-C relay module that can receive this max voltage and turn off and on depending on what signal is given.

Vrange: 0 - 3.5 Volts	This is the range of possible voltages that could be sent to the switch	I will be using the SRD-12VDC-SL-C relay module that can receive these range of voltages so that it knows when to turn on and off.
Other: Active High	When provided an active high of 3.5 volts. The switch will activate.	I will be using the SRD-12VDC-SL-C relay module that once sent a active voltage switches to shut off power

4.1.5 Verification Process

1. Plug in block to wall outlet.
2. Send a turn on signal to the switch to send power to each voltage regulator
3. Test pwr_plsm_gnrtn output maximum and minimum volatages.
4. Test pwr_plsm_gnrtn output nominal and peak currents
5. Test pwr_sgnl_prcssng_rcnstrctn output maximum and minimum volatages.
6. Test pwr_sgnl_prcssng_rcnstrctn output nominal and peak currents
7. Test pwr_wvfrm_gnrtn_mdltn output maximum and minimum volatages.
8. Test pwr_wvfrm_gnrtn_mdltn output nominal and peak currents
9. Send a off signal to the switch to shut off all power to system
10. Complete steps 3-8 to ensure no voltage or current is being outputed.

4.1.6 References and File Links

[1] Mulview, “500W single output switching power supply” S-500 series datasheet, Available: http://m.microjpm.com/_files/200006707-79dfe7ad65/S-500%20Series%20Datasheet.pdf [Accessed: 18-Fed-2022].

4.1.7 Revisions Table

Topic	Revision
Descriptions changed - 5/6/22	Updated descriptions and schematics to match most recent system.
Interface Properties - 3/4/22	Updated interface properties to make block diagram update
References changed 2/18/2022	Changed the reference to actual component being used

Additional information added 2/18/2022	Added specific components I will be using in the interface table.
Initial Doc Created 2/4/2022	Filled out complete document as a draft for revision

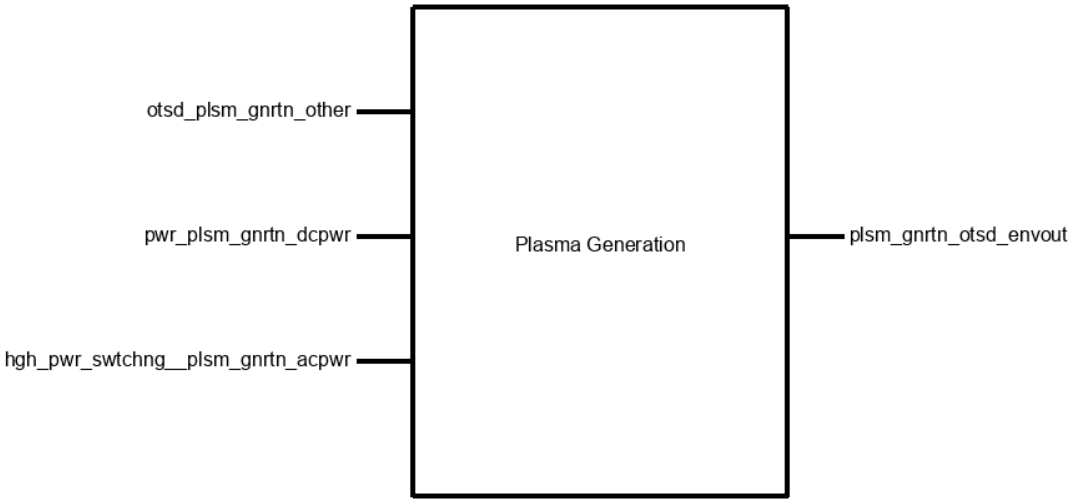
4.2 Plasma Generation

4.2.1 Description

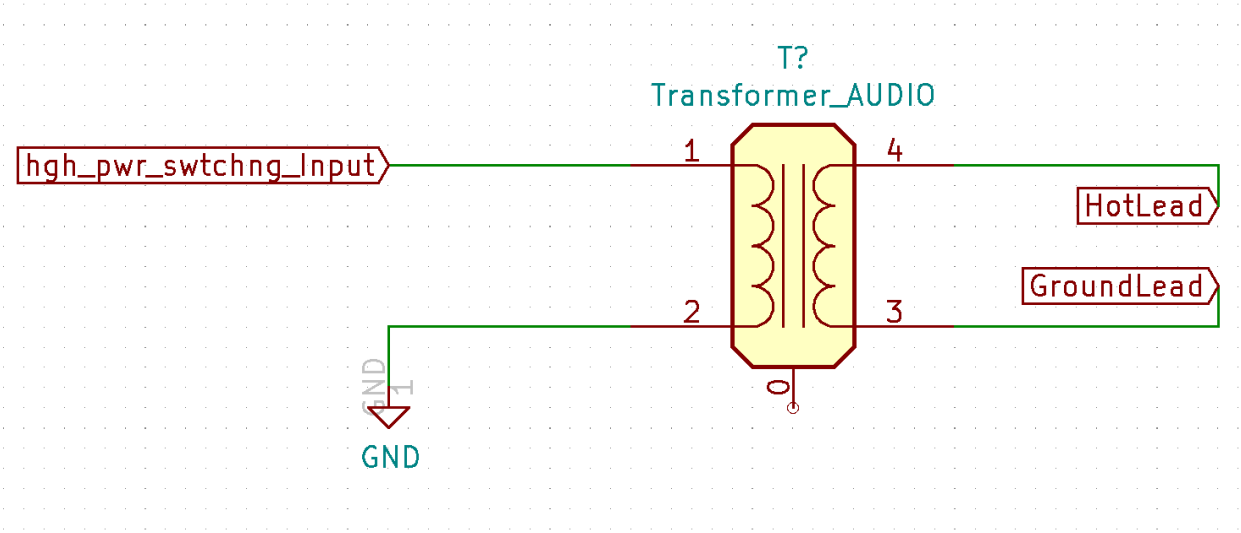
The Plasma Generation block consists of the transformer and electrodes used to amplify the voltage to create the electric arc. This is used to step up the voltage nearly 800 times for the electrodes. This block may also include large capacitors to speed up the circuit's transient response and provide instant voltage to the electrodes for the high-frequency sound signals.

4.2.2 Design

Black Box Diagram:



Schematic:



4.2.3 General Validation

The transformer will be able to step up the voltage high enough for an electrical arc to be produced. To produce an electric arc, the transformer must output more than 75,000 volts for our expected one-inch gap between the electrodes. The input voltage needs to be high enough so that the transformer can produce the needed 75,000 volts.[1]

4.2.4 Interface Validation

otsd_plsm_gnrtn_other : Input

Interface Property	Why is this interface this value?	Why do you know that your design details for this block above meet or exceed each property?
Other: Tubing Specification: 1/2" outer-diameter	This size of tubing allows for the right amount of helium to be present in the chamber.	The tubing specifications
Other: Concentration: 80%	This will allow the right amount of oxygen and helium so the arc can be activated	The helium is constantly being pumped into the closed chamber.
Other: Tubing Specification: 3/8" inner-diameter	This size of tubing allows for the right amount of helium to be present in the chamber.	The tubing specifications

Other: Type of Gas: Helium	Helium allows for a lower resistance for the arc to bridge	We will have a tank of helium pumping into out chamber

pwr_plsm_gnrtn_dcpwr : Input

Inominal: 3 Amps	The nominal current power is able to produce	With high voltage this current will provide enough Power to the transformer to produce an arc.
Ipeak: 4.5 Amps	The peak current power is able to produce	With high voltage this current will provide more than enough Power to the transformer to produce an arc.
Vmax: 20 Volts	The maximum Voltage power is able to produce	The transformer is able to step up a voltage by 800 Therefor with 20 Volts the transformer will be able to provide enough voltage to produce an electric arc
Vmin: 10.5 Volts	The minimum voltage power is able to produce	The transformer is able to step up a voltage by 800 Therefor with 10.5 Volts the transformer will be able to provide enough voltage to produce an electric arc

hgh_pwr_swtchng__plsm_gnrtn_acpwr : Input

Inominal: 1A	The nominal current high power switching is able to produce	With high voltage this current will provide enough Power to the transformer to produce an arc.
Vmax: 40 VAC	The maximum Voltage high power switching is able to produce	The transformer is able to step up a voltage by 800 Therefor with 40VAC the transformer will be able to provide enough voltage to produce an electric arc
Vmin: 24 VAC	The minimum voltage high power switching is able to produce	The transformer is able to step up a voltage by 800 Therefor with 24VAC the transformer will be able to provide enough voltage to produce an electric arc

plsm_gnrtn_otsd_envout : Output

Other: dBmin: 60 dB at 1 Meter	Average dB for a conversion at 1 Meter[2]	The high voltage charges the air around it and the switching current will expand and contract the air creating a sound higher than 60 dB.
Other: Voltage: 75,000 Volt min	It takes 75,000 Volts for electricity to jump an inch distance [1]	The transformer can be wound to produce a much higher voltage than this minimum.
Other: Frequency: 20K Hz to 35K Hz	To low of a frequency and the transformer doesn't work, to high of a frequency and not enough power to transformer.	Transformer needs switching current to operate and boost the voltage. The output frequency is the same speed as the input frequency.

4.2.5 Verification Process

1. Plug transformer into high power switching block and power block
2. Set inputs from power block to 3 amps and 10.5 volts
3. Set Inomial to 3 amp
4. Set input voltage to 20 Vac
5. Test/Verify a range of 20 - 35K Hz
6. Verify that noise level is above 60 dB at 1 meter away
7. Show arc is present verifying at least 75,000 volt output
8. Set input to 7.8 Vac
9. Do steps 4 - 6 again.
10. Set inputs from power block to 4.5 amps and 20 volts
11. Do steps 3 - 9 again.

4.2.6 References and File Links

[1] K. Wallewein, "How many volts does it take for electricity to ... - quora," *Quora*, 2018. [Online]. Available: https://www.quora.com/How-many-volts-does-it-take-for-electricity-to-jump-to-another-metal-object. [Accessed: 07-Jan-2022].

4.2.7 Revisions Table

Topic	Revision
Interface Properties - 3/4/22	Updated interface properties to make block diagram update
Verifican plan - 1/21/22	Rewrote plan to test all possible input/output combinations.
Schematic changed - 1/21/22	Changed schematic to only represent my block.
Interface properties changed - 1/21/22	Conversed with Don and my team to define testable outputs for my block and changed them in the table.
Document Finalized - 1/7/22	Added references, and reformatted documents.
Content Added - 1/5/22	Added content to Verification Plan, Interface Validation, General Validation, and Design Sections.
Initial Document Created - 1/5/22	Copy and paste from the online tool.

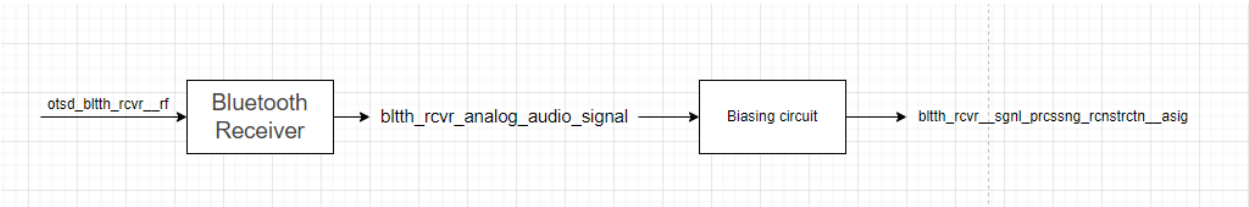
4.3 Bluetooth

4.3.1 Description

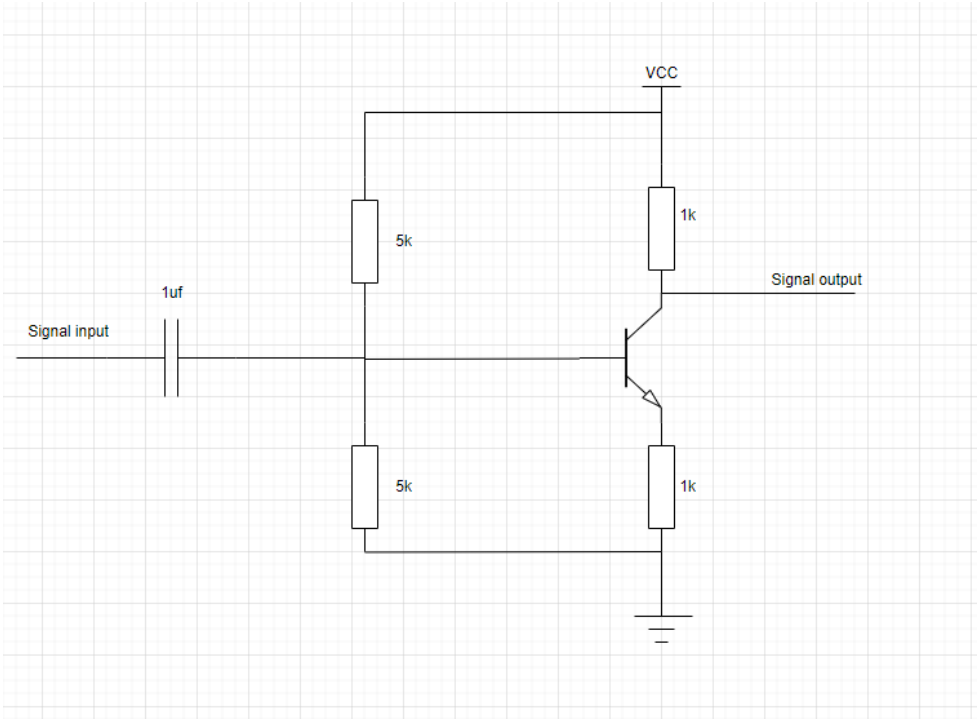
The Bluetooth receiving module includes a Bluetooth audio module and a bias circuit. The Bluetooth audio module uses A2DP protocol to communicate with external Bluetooth signals and decodes audio data to generate audio analog signals. The bias circuit then biases the audio signal to produce a bias signal consistent with the sampling of the post-stage ADC.

4.3.2 Design

Block diagram:



Schematic Diagram: Bias circuit



External Bluetooth signals are received by Bluetooth audio module, analyzed by on-chip protocol, decoded by audio, and finally output as analog signals through DAC. The bias circuit biases the generated analog signal and provides gain appropriately, so that the signal can maximize the coverage of sampling range, improve sampling accuracy.

4.3.3 General Validation

Verify that the Bluetooth audio module can be stably paired with external Bluetooth devices.

Verify that the Bluetooth audio module can send data according to the specified protocol and can decode it correctly
a bias circuit can add dc bias to the audio signal and provide appropriate gain
The rear ADC sampling can correctly sample the analog signal output from the bias circuit.

4.3.4 Interface Validation

Interface Property	Why is this interface of this value?	Why do you know that your design details <u>for this block</u> above meet or exceed each property?
otsd_bltth_rcvr__rf		
External Bluetooth signal protocol	A2DP Protocol	The module supports the universal Bluetooth audio protocol
Host input source data format	WAV/MP3	Common audio formats that are resolvable by the module protocol
Bias circuit signal output	Vmin: 0V Vmax: 5V Imin: 0 mA Imax: 10 mA	According to the data manual of the rear stage module, the input voltage range is between 0V and 5V, and the driving current is less than 10mA, which meets the electrical requirements of the rear DAC driver

The Bluetooth audio module can receive an external Bluetooth signal and generate an analog signal.

The bias circuit provides the correct bias and amplifies the signal appropriately.

4.3.5 Verification Process

1. External devices can be paired with Bluetooth audio modules
2. The Bluetooth audio module relates to a small speaker to play music normally

3. Measure the output waveform amplitude of the bias circuit within the input range of the rear ADC
4. Test bias circuit with standard source can provide bias and gain normally
5. Joint adjustment with the post-stage signal processing unit

4.3.6 References and File Links

Data sheet about Bluetooth receiver:
https://www.amazon.com/MakerHawk-Bluetooth-Receiver-Amplifier-Speaker/dp/B08D94PGCG/ref=sxin_14_ac_d_bv?ac_md=0-0-QmVzdCBWYWx1ZQ%3D%3D-ac_d_bv_bv_bv&crid=GKJTR9OP03VL&cv_ct_cx=bluetooth%2Bchip&keywords=bluetooth%2Bchip&pd_rd_i=B08D94PGCG&pd_rd_r=92eb7a4e-fb36-422f-b9f3-c0a4efb74fa5&pd_rd_w=WhDwn&pd_rd_wg=DFMXV&pf_rd_p=148e9898-1bed-4a70-9840-46f32e4185bd&pf_rd_r=JPJ5CPRRDQRFWCN8FSN1&qid=1641618998&sprefix=bluetooth%2Bchi%27p%2Caps%2C152&sr=1-1-f4ff053e-b1e8-4d31-8f95-56d755c862ba&th=1

4.3.7 Revisions Table

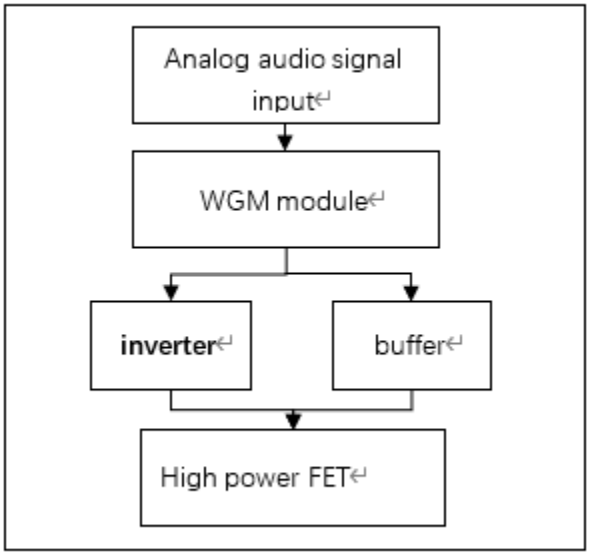
Date	Topic	Revision
2022/1/20	Reword some details	Re-do block diagram, and rewrite interface validation and verification plan.

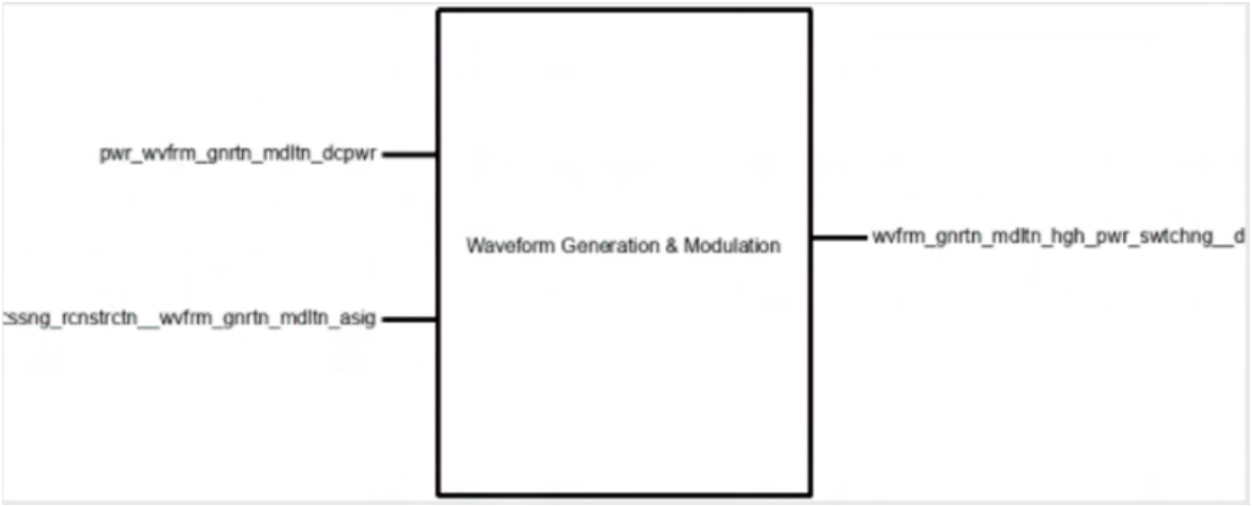
4.4 Waveform Generation Modulation

4.4.1 Description

Taking the analog audio signal as an input, the WGM block will modify the duty cycle of a square wave. This modulation is what implants the audio within the eventual high-power signal. The modulated square wave is then split into a buffer and an inverter to create mirrored signals perfectly in phase. This is used to create the push-pull characteristics needed to sustain high voltage. This will be implemented with 3 different integrated circuits, one for pulse width modulation, one buffer, and one inverter.

4.4.2 Design

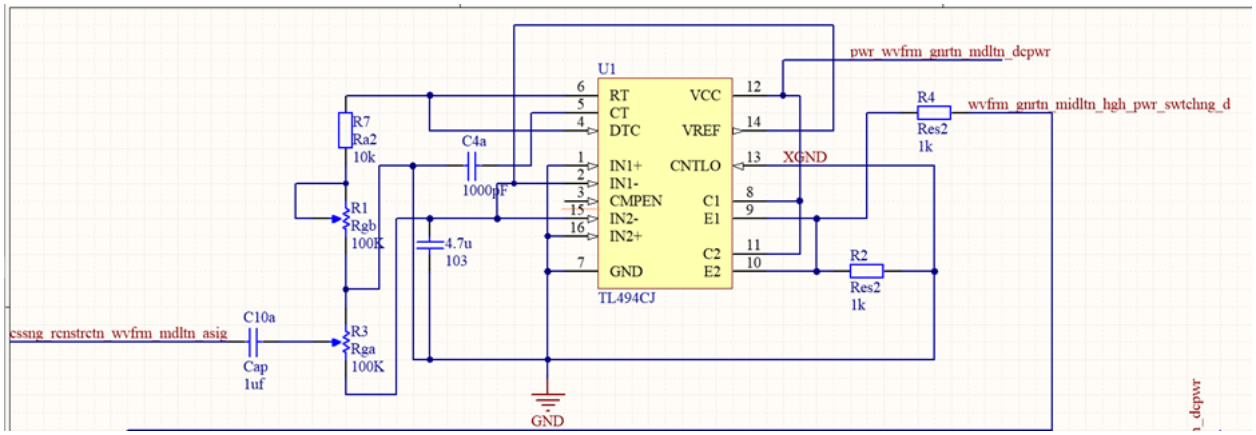




The WGM module is depicted above, and the upper left port is a DC input module with a 5V supply voltage to power the circuit. And the left bottom port is a signal following signal preprocessing; audio frequency modulation is accomplished by continually modifying the duty ratio of the PWM wave; and the right port is an output modulated square wave. Through a buffer and an inverter, the modulated PWM wave generates a mirror image signal with the same phase. The two output signals combine to generate a push-pull circuit that powers the IRFP260N. The innovation has the advantages of high output power and low heat generation while maintaining the push-out characteristic required by high voltage, and it can respond fast to the driving signal, allowing for a good restoration of the audio signal.

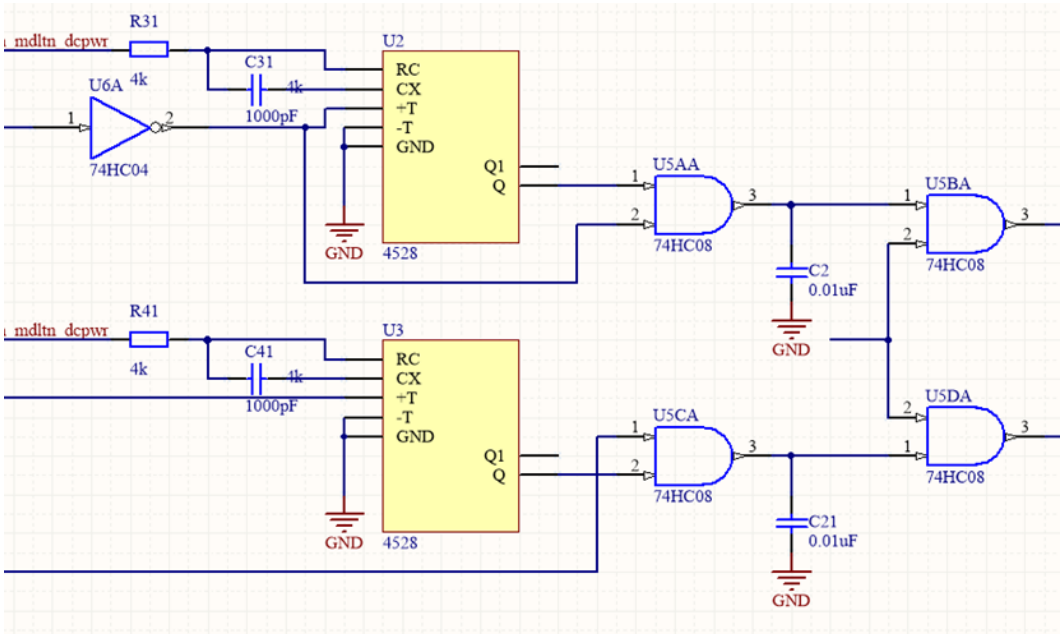
4.4.3 General Validation

4.4.3.1 PWM Modulation Module



The module binds the pre-processed audio to the TL494's fourth pin via a capacitor and then modifies the fourth pin's voltage to affect the pulse width, so altering the temperature of the ion body and generating sound. The module employs a MOS single tube driving mode; the thirteenth pin of the TL494 is grounded, namely, the 12th pin is at a low level, and the output waveforms of the two triodes in the TL494 are consistent, allowing for control of the PWM waveform produced by the MOS hard switch's output modulation.

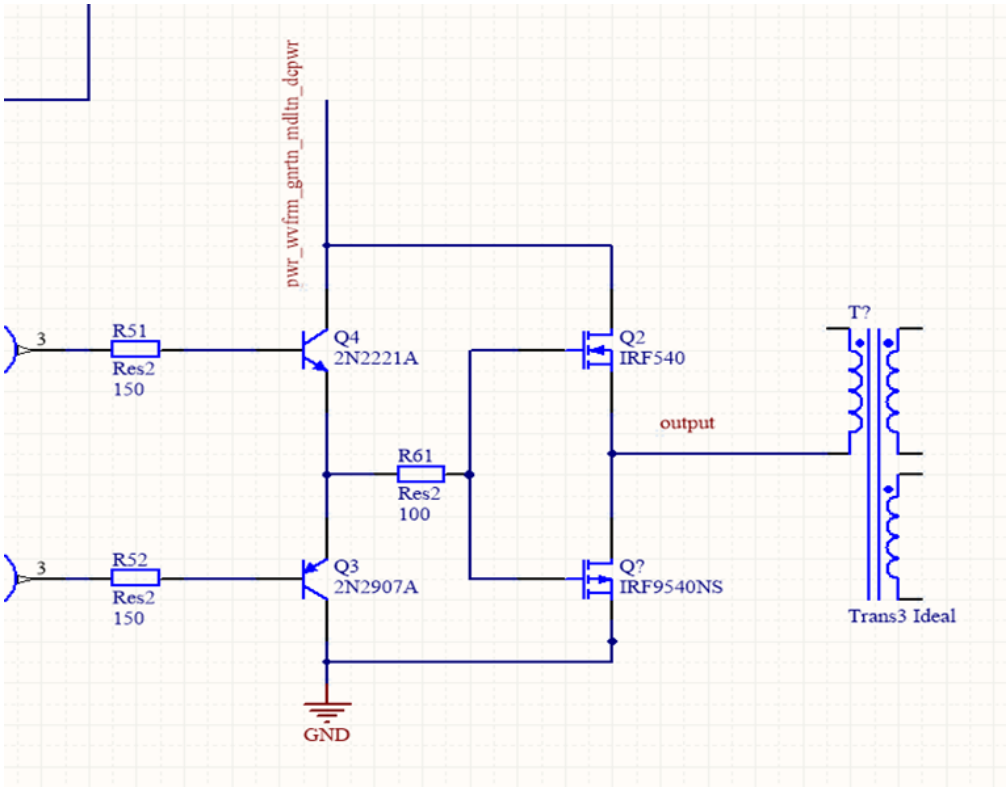
4.4.3.2 Inverting and buffering module



The inversion module is based on the 74HC04 logic element, while the buffer module is based on the CC4528, which has the purpose of preventing the microswitch from shaking and

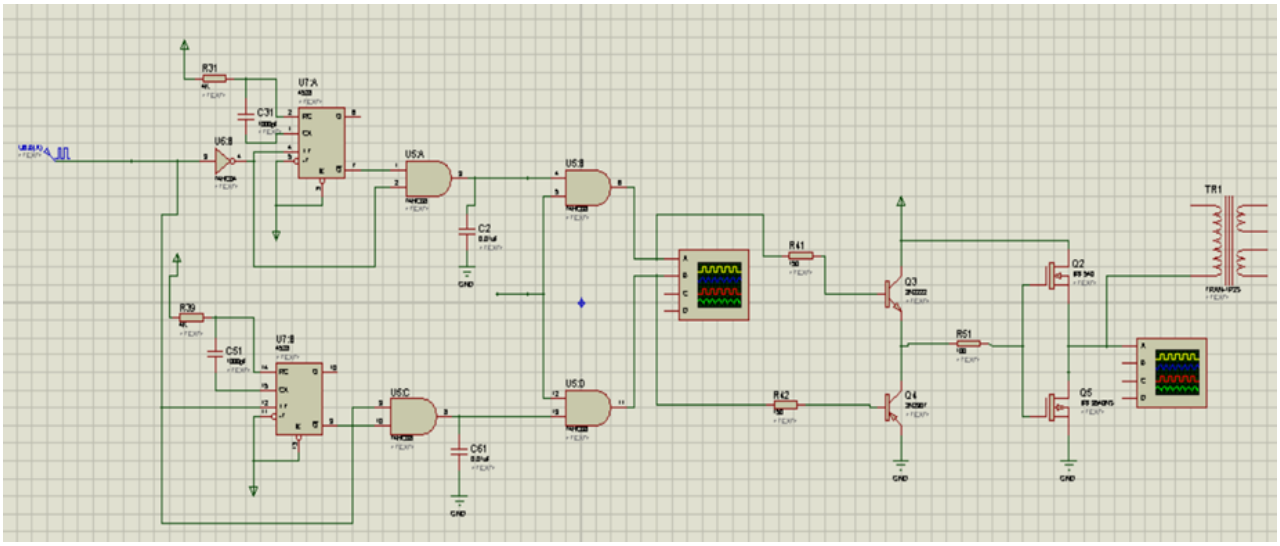
delaying, as well as efficiently triggering the MOS tube. and after passing through the 74HC04, outputting two lines of mirror image PWM waveforms to be used as driving signals for the MOS tubes in the circuit.

4.4.3.3 Drive Circuit

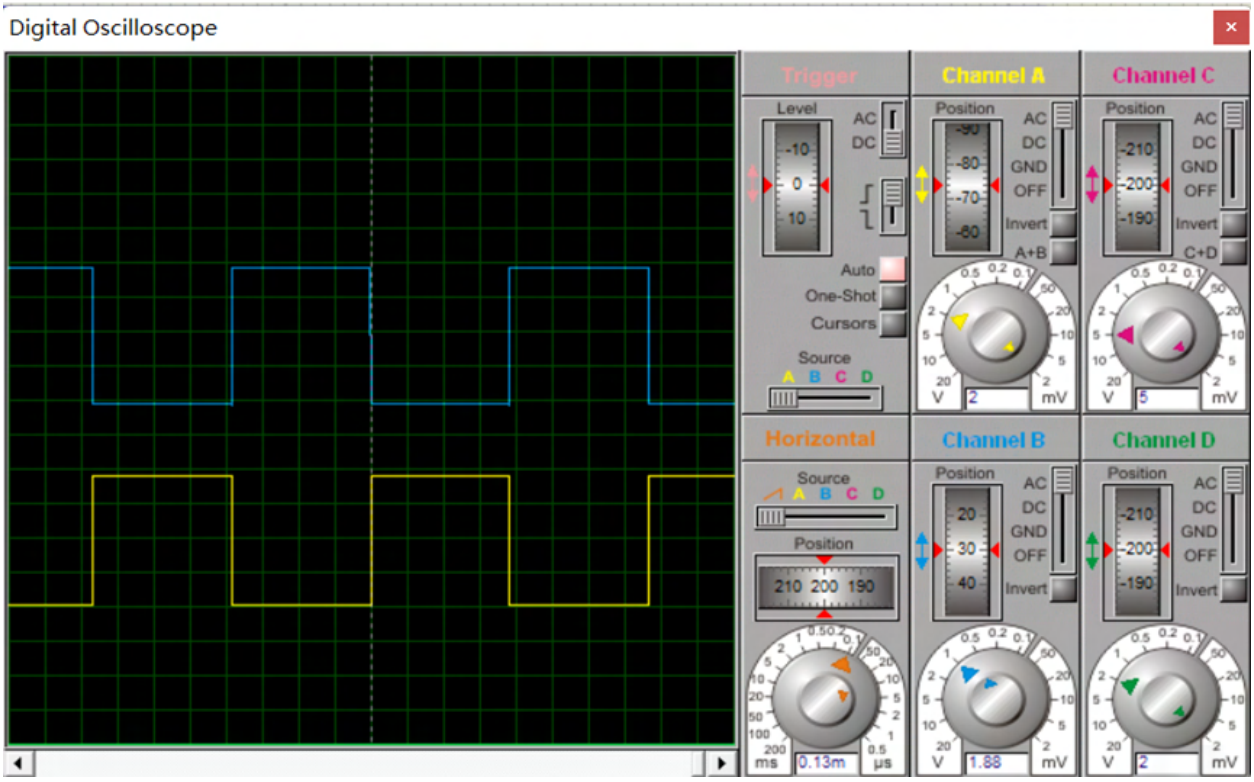


As illustrated in the figure above, the inverse buffer module's control signal has a high output voltage and a low current, necessitating the use of a MOS tube with a low GS capacitance to minimize damage to the MOS tube and triode. Two triodes are used in the module circuit to drive the N-type MOS and the P-type MOS, forming a GS capacitor discharge circuit that accelerates the MOS turning-off while minimizing switching loss.

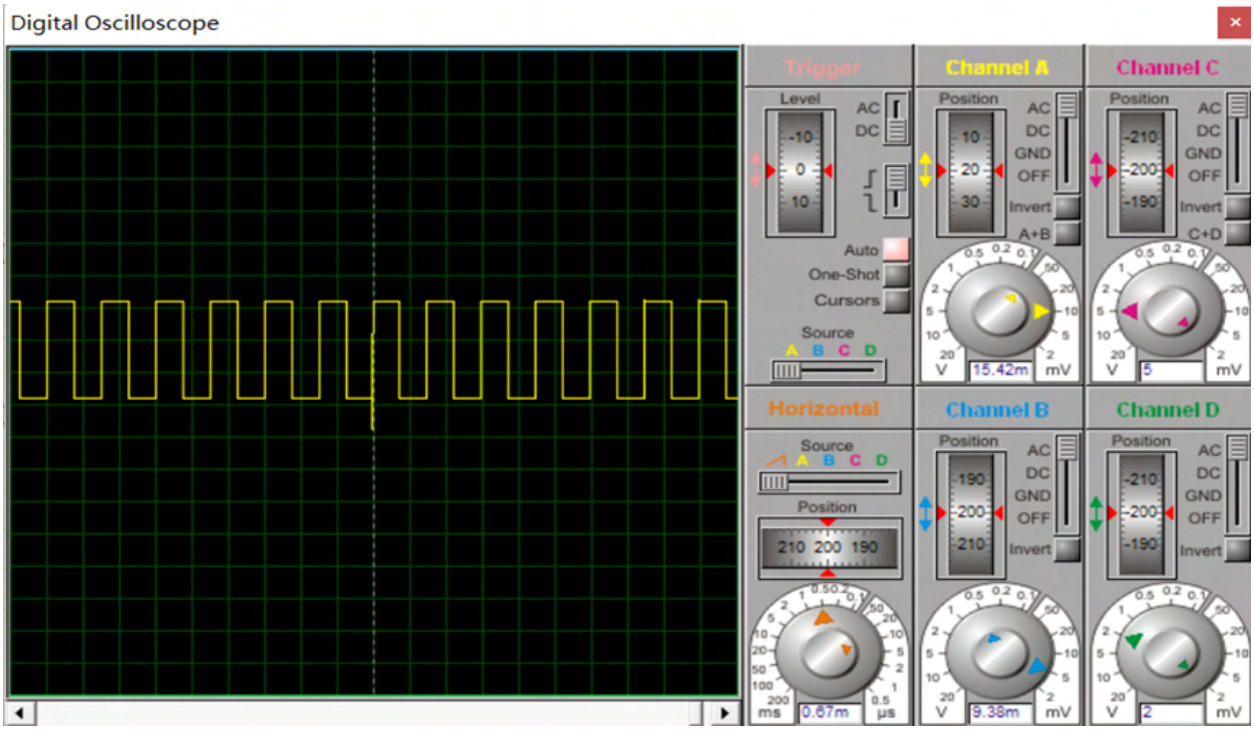
The PWM inverter, buffer and drive circuits are verified by protues software. A simulation circuit is established as follows:



The above test circuit accepts a PWM signal and simulates an audio waveform modulated by the TL494. The output of one path is inverted and delayed, while the output of the second path is buffered and delayed driving Q3 and Q4, respectively.

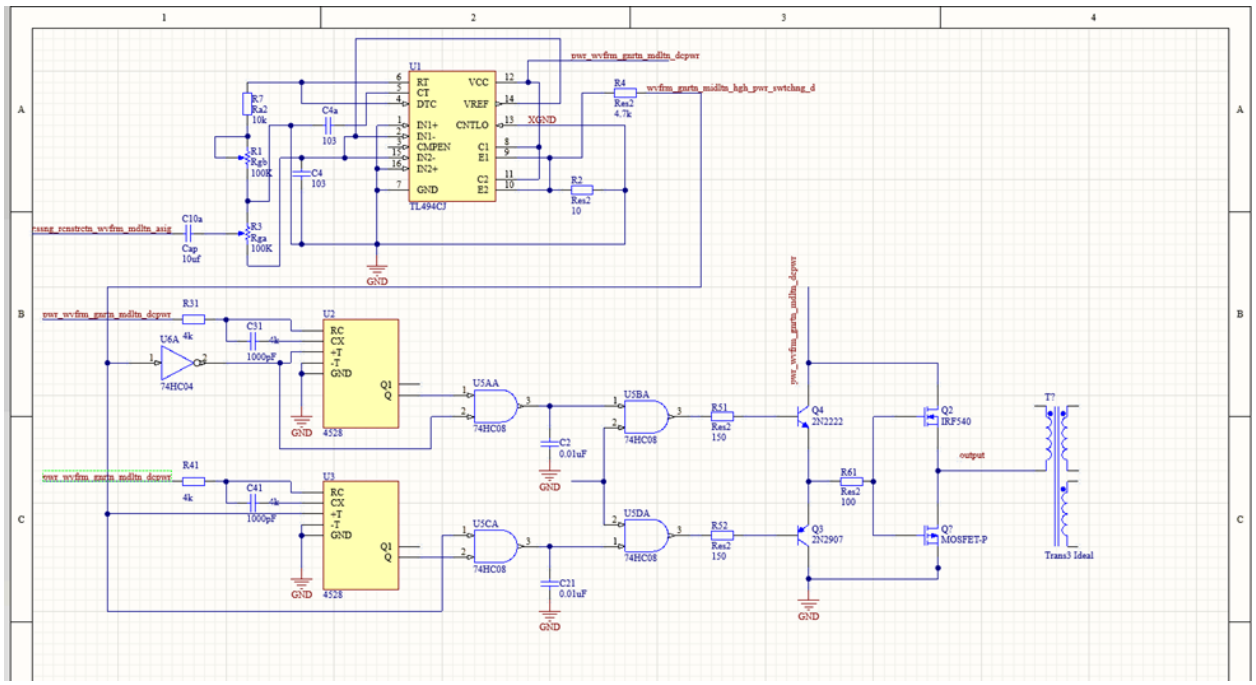


The above figure shows the two output waveforms after inversion and buffering, and it can be seen from the figure that the output is a mirror PWM waveform, which meets the expected design requirements.



The above diagram shows the PWM waveform generated when the MOS is turned off after the MOS transistor is driven to operate, and the output is sent to the transformer.

4.4.3.4 Whole Circuit



4.4.4 Interface Validation

pwr_wvfrm_gnrtn_mdltn_dcpwr : Input

Ipeak: 2 Amps	This is the peak current used by the components in this block.	In the circuit, I designed a sliding rheostat, which can adjust different currents according to different voltages, so 2A is feasible.
Vmax: 5 Volts	This is the maximum voltage needed to ensure components are provided enough power to work.	The circuit can pass the voltage of 5V, through the sliding rheostat adjustment, can realize the corresponding current

sgnl_prcssng_rcnstrctn__wvfrm_gnrtn_mdltn_asig : Input

Max Frequency: 20K Hz	Common upper range of human hearing	PWM is a modulation module that can be adjustable at 100KHZ, so 20K Hz can be realized.
Vmax: 1.5V	Maximum output for DAC	According to the test, the circuit satisfies this input
Vrange: +-1V	Input range for IC and used for WGM block	According to the test, the circuit satisfies this input

wvfrm_gnrtn_mdltn_hgh_pwr_swtchng__dsig : Output

Logic-Level: 10V	TL494 PWM control chipset is used to create the PWM signal that drives the gate of the MOSFET and the switching action. The datasheet lists the maximum collector output voltage (output signal) as 41V. Thus, 10V falls easily below this and within spec for the chipset.	After multimeter testing, the circuit can output this value and can drive the MOSFET gates.

Other: Fmin=8KHz	Next part requirement	Use oscilloscope, according to the tests, square waves can be generated at this output
Other: Fmax=25KHz	Next part requirement (the frequency is because the square wave signal is modulated again with PWM so it needs to be high enough to be cut down further)	Use oscilloscope, according to the tests, square waves can be generated at this output

4.4.5 Verification Process

1. Use multimeter, test the circuit, when the current is 2A, what is the voltage

2. Test the circuit, when the voltage is 5V, what is the current

3. Test whether 20KHz can work when PWM is connected to signal processing module, and test Vmax and Vrange

4. When the circuit is connected to the power supply, test whether the output is 10V

5. Use oscilloscope, test the waveform, when the minimum frequency is 8KHz and the maximum frequency is 25KHz, whether the square wave can be realized

4.4.6 References and File Links

IRFP260N MOSFET Datasheet - link

TL494 PWM Control Chipset Datasheet - link

74HC04 logic elements:
https://www.digikey.com/htmldatasheets/production/2095793/0/0/1/74hc-t-04.html?utm_adgroup=xGeneral&utm_source=google&utm_medium=cpc&utm_campaign=Dynamic%20Search_EN_Product&utm_term=&utm_content=xGeneral&gclid=Cj0KCQiApL2QBhC8ARIsAGMm-KFnXfetWD-pyaLK1-bqlz118TPv0usLSbcQiVzuh9RybzMxyJFQnnAaAvvrEALw_wcB

CD4528 buffer Datasheet: https://www.futurlec.com/4000Series/CD4528.shtml

4.4.7 Revisions Table

Date	Topic	Revision
2022/2/4	Initial Draft	Initial Draft by Zhenglun Yang and will update some details after circuit design completed
2022/2/18	Second Draft	Add circuit diagram and schematic, add some info.

4.5 High Power Switching

4.5.1 Description

The outputs from the Waveform Generation and Modulation block are not capable of providing enough power to the transformer to create the electrical arc. Thus those signals are instead fed into the High Power Switching block which steps up the PWM signal to a higher voltage using a power MOSFET. This higher voltage signal is then inputted into the transformer, creating enough voltage to initiate the electrical arc. The High Power Switching block requires high voltage DC power from the system's Power Block in order to drive the MOSFET. The high power switching uses a single n-channel MOSFET as a low-side driver to sink current down through the transformers primary coil. This provides a single ended (single direction) high voltage and high current signal to the transformer. Additional protection and filtering components are necessary to support the MOSFET as well as heatsinks and careful thermal considerations.

4.5.2 Design

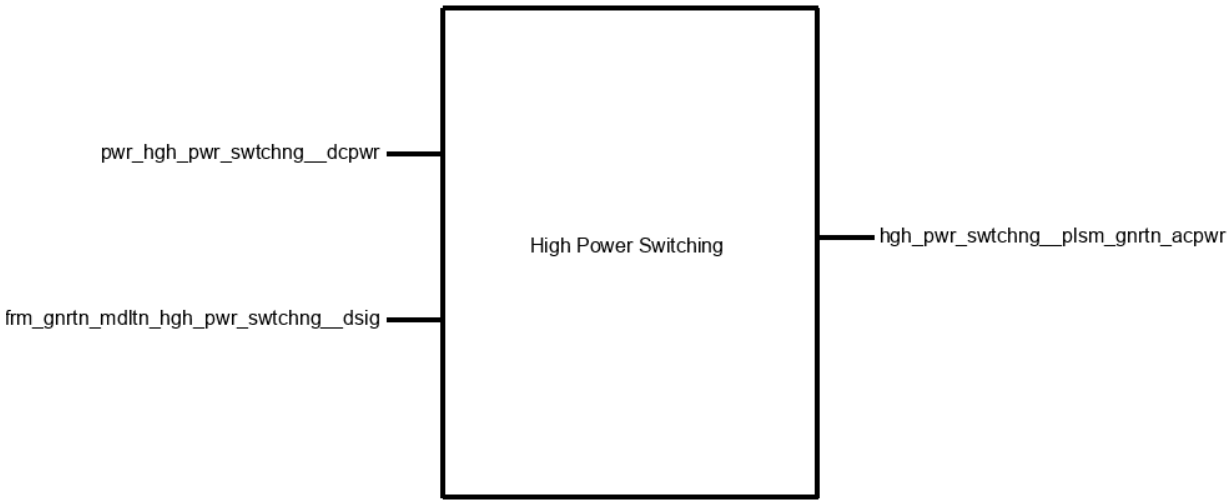


Figure 4.5.1: High Power Switching Black Box Diagram

Figure 1 above shows the black box diagram for the High Power Switching block. The *pwr_hgh_pwr_swtchng_dcpwr* input is the DC power input that supplies power to the MOSFET. The *frm_gntn_mdltn_hgh_pwr_swtchng_dsign* input is the PWM input from the Waveform Generation and Modulation Block that encodes the audio signal for the speaker. The *hgh_pwr_swtchng_plsm_gnrtn_acpwr* output is the amplified PWM output signal that gets sent through the primary winding of the transformer. This output signal gets stepped up again by the transformer in the Plasma Generation block and directly creates the plasma arc for the speaker.

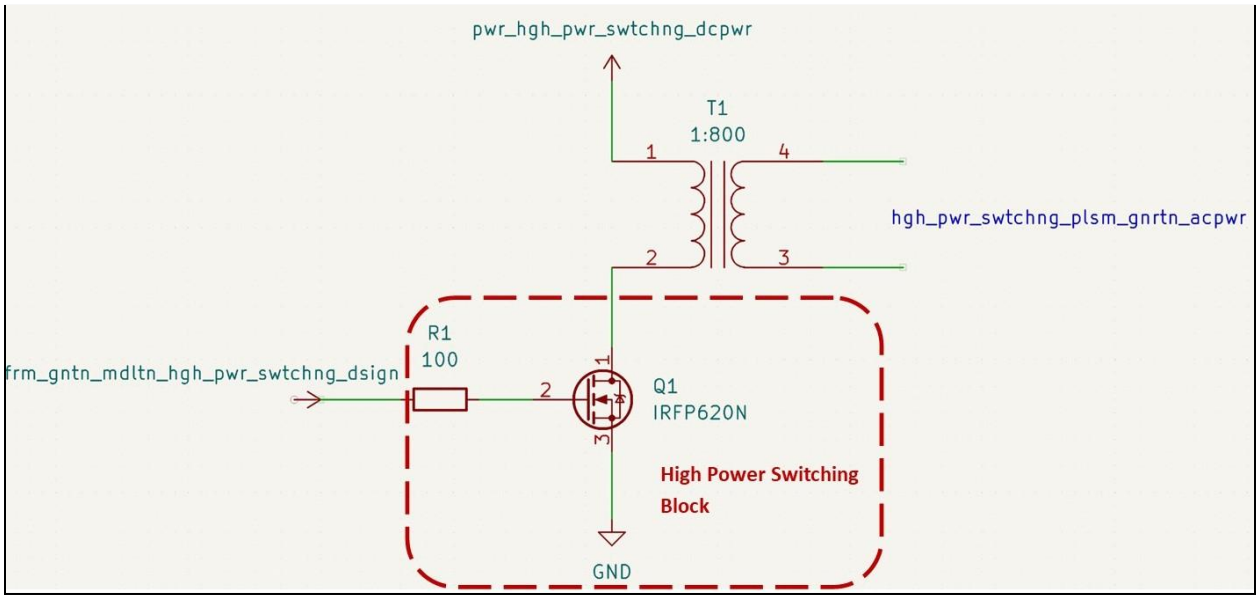


Figure 4.5.2: High Power Switching Schematic with System

Figure 2 above shows the High Power Switching block outlined in red. The block is shown with the transformer for better clarity of system flow. The final design of the block converged to a single low-side NMOS MOSFET driver to pull current through the transformer. A high voltage power rail is connected to the high side of the primary coil in the transformer, and thus the drain of the MOSFET. The 12V PWM input signal is connected to the gate of the MOSFET, switching the device on and off. When the input signal is high, the Vgs threshold voltage of the MOSFET is exceeded and the device switches to the triode region of operation and conducts the current through the transformer to ground. When the PWM is low, the Vgs threshold for the device is not exceeded and it acts as an open circuit, thus not allowing any current to flow through the transformer.

A low-side design was selected instead of a high-side design (PMOS transistor above the transformer, with source connected directly to the supply) due to the nature of the PWM input signal. If a PMOS high-side MOSFET was used, the gate voltage would need to be higher to best control the Vov of the MOSFET because the Vgs is referenced off the supply voltage.

The 100Ohm resistor on the MOSFET gate is to reduce parasitic oscillations that occur due to the MOSFETs input capacitance combined with the input circuitry's inductance. This slows down the turn-on time of the MOSFET and causes excess current to flow through the drain/source impedance.

MOSFET: IRFP260N

Resistor: 100Ohm, 5W

4.5.3 General Validation

3.1 MOSFET Verification

The power FET for the block was selected based on voltage and current ratings as well as timing and thermal properties. Calculations done with the transformer and voltage requirements/impedances for electrical arcing showed that the MOSFET needed to create a voltage between 24 and 40V. Thus the maximum Vds tolerance of the transistor needed to be well above this to work most efficiently. Along with the high supply voltage, switching transformers often cause voltage spikes due to the inductive nature of their coils. A voltage rating of >100V was desirable. The IRFP260N MOSFET has a Vds voltage rating of 200V, giving plenty of headroom.

The Ids current tolerance of the MOSFET was also important. Although the actual current through the MOSFET while in use is highly dependent on the transformer load, a very high 5A peak current was identified. The IRFP260N MOSFET has a continuous Idc current rating of 50A at 10V Vgs, again giving plenty of headroom.

The next main requirement for the MOSFET was switching speed. Our speaker system is set to use a frequency less than a maximum of 50KHz, thus the MOSFET would have to support this.

Simple math shows that the maximum allowed total switching time for the MOSFET would be 20microseconds. This includes turn-on delay, rise time, turn-off delay, and fall time. Table 1 below shows the timing specs from the IRFP260N MOSFET datasheet. The total switching time is calculated to be 180ns or 0.18microseconds. Thus allowing for the MOSFET to switch at an ideal 5.5GHz. Even considering parasitics that would cut this nearly in half, the MOSFET still gives plenty of headroom for our application.

$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 100V
t_r	Rise Time	—	60	—		I_D = 28A
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		R_G = 1.8Ω
t_f	Fall Time	—	48	—		V_{GS} = 10V ④

Table 4.5.1: IRFP260N Timing Specs

The last main requirement for the MOSFET is the thermal and power requirement. The main contributor to MOSFET thermal issues is the drain/source impedance which burns power when the device is switching between on and off. The equation to estimate this power dissipation for a switching MOSFET is as follows:

$$P_{DSWITCHING} = (C_{RSS} \times V_{IN}^2 \times f_{SW} \times I_{LOAD})/I_{GATE}$$

Plugging in values from the IRFP260N datasheet and nominal output/input currents and voltages at 50Khz gives a value of 5.29Watts of power dissipation. The IRFP260N is rated to 300W, with a linear derating factor of 2 W/degreeC. Thus even as the device heats up, the power dissipation will reach nowhere near the maximum rated value.

Other important aspects of the MOSFET for our application are the Vgs tolerances and the diode protection. The IRFP260N has a maximum Vgs voltage of 20V, giving our 12V PWM input signal a significant amount of headroom. The IRFP260N MOSFET also includes a convenient body diode shown as a protection measure against reverse current.

In conclusion, the IRFP260N MOSFET exceeds all of the necessary requirements and was chosen for the design.

The chosen single MOSFET design leads to much easier testing and construction of the circuit as well as a simplified process of sourcing components. With only one MOSFET acting as a switch, the circuit can be constructed for testing on a protoboard or even wired together. This leads to faster turnarounds for testing and allows the team to further design and test the rest of the system. Along with this, any errors or problems that do occur can easily be troubleshooted due to simple signal flow through the circuit. While a single MOSFET design is less technically astounding, the time saved on sourcing, testing, and constructing the circuit will be put to better use in other aspects of the system design, leading to a more refined final product. Component availability is also restricted as specific high power MOSFETs are available only online, with an average of 2-week shipping time. The selected IRFP260N MOSFET is already on hand and ready to be tested.

4.5.4 Interface Validation

Interface Property	Why is this interface this value?	Why do you know that your design details for this block above meet or exceed each property?
pwr_hgh_pwr_swtchng__dcpwr : Input		
Inominal: 1 Amp	1A DC at the Vmin of 24V gives 24W of power, and gives 40W of power at the Vmax of 40V. Using the known 1:800 ratio of the flyback transformer and the transformer output voltages calculated below, this leads to a transformer output current of 1.25mA at both Vmin and Vmax. This is above the current threshold for both output voltages to produce an electrical arc of the desired length. Electrical arcs are produced mainly due to high voltage potential differences, thus the current values do not need to be high.	This current gets sunk through the drain of the MOSFET. The IRFP260N MOSFET has a continuous current rating of 50A at 25C, and 35A at 100C. The datasheet also lists the maximum pulsed drain current at 200A. Thus even at high temperature, 1A of current is far below the maximum threshold for the device.
Ipeak: 5 Amps	Flyback transformer used in the design is rated to 220W as per labeling on the component. Although 5A is likely never going to be drawn continuously, a current spike caused by the inductance of the switching transformer could lead to a momentary 4-5A. At the Vmax listed below of 40V, 5A of current leads to a transient power draw of 200W, thus not exceeding the transformers rating at the worst possible conditions.	This current gets sunk through the drain of the MOSFET. The IRFP260N MOSFET has a continuous current rating of 50A at 25C, and 35A at 100C. The datasheet also lists the maximum pulsed drain current at 200A. Thus even at high temperature, 5A of current is far below the maximum threshold for the device.
Vmax: 40 Volts	40V DC power into the transformer and drain of the	This signal is connected to the MOSFET drain, and the

	MOSFET lead to a maximum transformer output voltage of 32kV based on the 1:800 ratio. Calculations based on the impedance of electrical arc and desired arc length show that 32kV is enough potential to produce a 4cm arc through typical air.	IRFP260N MOSFET Vds is rated to a maximum of 200V as per the datasheet. Thus the 40V drain voltage is far below the maximum threshold for the device.
Vmin: 24 Volts	24V DC power into the transformer and drain of the MOSFET lead to a maximum transformer output voltage of 19.2kV based on the 1:800 ratio. Calculations based on the impedance of electrical arc and desired arc length show that 19.2kV is enough potential to produce a 3cm arc through typical air.	This signal is connected to the MOSFET drain, and the IRFP260N MOSFET Vds is rated to a maximum of 200V as per the datasheet. Thus the 24V drain voltage is far below the maximum threshold for the device.

hgh_pwr_swtchng__plsm_gnrtn_acpwr : Output

Inominal: 1 Amp	1A nominal was chosen as per calculations shown in pwr_hgh_pwr_swtchng__dcpwr : Input property description above.	Because of the layout of the circuit, the low-side MOSFET pulls all of the current from the DC power input through the transformer primary coil (this output). Thus the Inominal input current is equal to the Inominal current through the transformer.
Vmax: 40 VAC	40Vmax input voltage was chosen as per calculations shown in pwr_hgh_pwr_swtchng__dcpwr : Input property description above. The MOSFET simply applies the PWM waveform to the input voltage, leading to an AC waveform of the same magnitude.	Because the input DC voltage source is above the transformer, the maximum voltage is applied directly to the transformer (this output). When the MOSFET switch acts as closed, there is ideally no voltage drop through the transformer because it is only a coiled wire. Thus the input DC voltage will remain at the same voltage level, but will be turned

		into an AC signal through the switching action of the MOSFET.
Vmin: 24 VAC	24Vmin input voltage was chosen as per calculations shown in pwr_hgh_pwr_swtchng__dcpwr : Input property description above. The MOSFET simply applies the PWM waveform to the input voltage, leading to an AC waveform of the same magnitude.	Because the input DC voltage source is above the transformer, the minimum voltage is applied directly to the transformer (this output). When the MOSFET switch acts as closed, there is ideally no voltage drop through the transformer because it is only a coiled wire. Thus the input DC voltage will remain at the same voltage level, but will be turned into an AC signal through the switching action of the MOSFET.

wvfrm_gnrtn_mdltn_hgh_pwr_swtchng__dsig : Input

Logic-Level: 12V	The TL494, and TC4429 PWM control chipset is used to create the PWM signal that drives the gate of the MOSFET and the switching action. The datasheet lists the maximum collector output voltage (output signal) as 41V. Thus 10V falls easily below this and within spec for the chipset.	This signal directly drives the IRFP260N MOSFET gate. The datasheet lists the Vgs maximum voltage as 20V. The source of the device is tied to ground, thus leading to a Vgs of 10V, falling within spec for the device. The Threshold voltage for the device is listed on the datasheet as 2Vmin and 4V max depending on the operating conditions. A 10V Vgs exceeds this and thus will be able to switch the device on under any condition. The 10V also gives ample overdrive voltage, leading to the threshold voltage being exceeded quickly and aiding in reducing switching delays.
Max Frequency: 50K Hz	The TL494, and TC4429 PWM control chipset is used to create the PWM signal that drives the gate of the MOSFET and the switching action. The datasheet	Table 1 in the document above shows the IRFP260N MOSFET switching times as per the datasheet. Combining the turn-on delay, rise time, turn-off delay, and

	lists the minimum operating frequency as 1kHz, and the maximum as 300kHz, thus 50kHz falls within the operating range for the chipset. This signal also creates the audio from the electrical arc and anything above 30kHz is outside of the human ear detection range. Thus after non-idealities in the switching and PWM distortion, the 50kHz maximum leaves us plenty enough headroom to reach the highest audible frequencies for the speaker.	fall time of the device leads to an ideal maximum switching frequency of 5.5GHz. Thus allowing the device to easily switch at 50kHz with minimal distortion.

4.5.5 Verification Process

1. Set up circuit on protoboard as seen in figure 2 above. Connect the function generator to the circuit input in place of the wvfrm_gnrtn_mdltn_hgh_pwr_swtchng__dsig signal. Set the function generator to square wave, 12V.
2. Connect MOSFET drain to an oscilloscope, set function generator input to 50kHz, set DC power input to 40V. Observe switching square waveform on oscilloscope, verifying wvfrm_gnrtn_mdltn_hgh_pwr_swtchng__dsig maximum frequency, logic level, and hgh_pwr_swtchng__plsm_gnrtn_acpwr Vmax. Repeat with supply voltage at 24V, verifying hgh_pwr_swtchng__plsm_gnrtn_acpwr Vmin. This also confirms pwr_hgh_pwr_swtchng__dcpwr Vmax and Vmin.
3. Connect the multimeter in series with MOSFET drain (making sure the multimeter is on the fused setting and the voltage rating exceeds supply voltage). Observe current, verifying verifying hgh_pwr_swtchng__plsm_gnrtn_acpwr Inominal and pwr_hgh_pwr_swtchng__dcpwr Inominal.

4.5.6 References and File Links

IRFP260N MOSFET Datasheet - link

TL494 PWM Control Chipset Datasheet - link

Schematic Files - link

4.5.7 Revisions Table

Date	Topic	Revision
1/21/2022	Verification Plan	Completed verification plan to test and verify each interface and the corresponding properties.
1/21/2022	Interface Validations	Completed interface validations for finalized interface properties.
1/20/2022	Schematic and Description	Added block schematic and accompanying description for design.
1/20/2022	MOSFET Validation	Added MOSFET validation for the chosen IRFP260N N-channel MOSFET.
1/20/2022	Major Design Revision	A simpler single MOSFET design was chosen by the team in place of the full-bridge double-ended output design.
1/20/2022	Introduction Updates and Revisions	Make the inputs/outputs clearer as per recommendation by Shelby Westerberg.
01/07/2022	Initial Draft	Initial draft was created with design ideas and plans/requirement for future developments

4.6 Enclosure

4.6.1 Description

This block is the physical enclosure for the entire Electrical Arc Speaker system. This includes the mounting and layout of all the various subsystems and the display of the arc-emitting electrodes. The enclosure block will also include safety precautions such as limiting how close a user can get to the plasma arc and being constructed of a non-conductive material. Along with this, the enclosure will be aesthetically pleasing, mechanically sturdy, and facilitate the speaker system's ability to connect to the end-user. This enclosure is designed for the speaker to be a desktop sized object, around 30cm tall and 25x21cm at the base.

4.6.2 Design

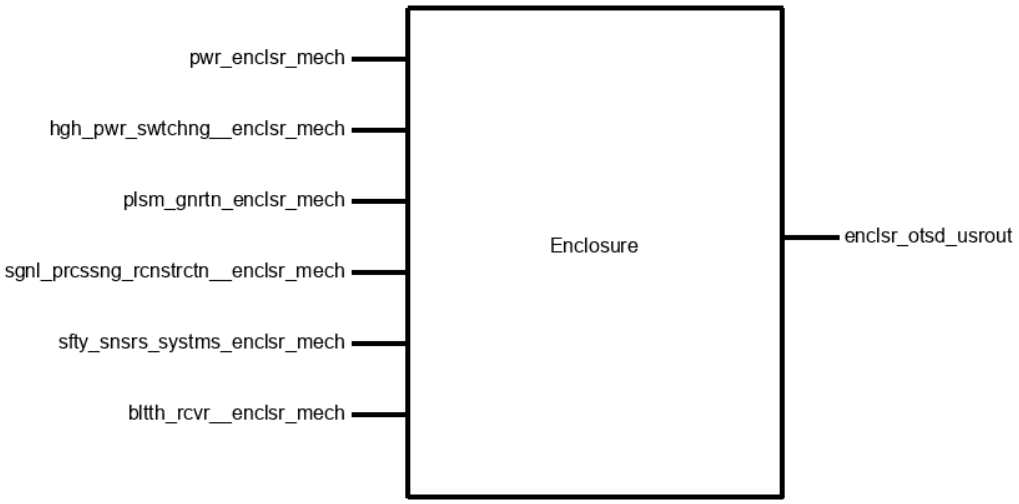


Figure 4.6.1: Black Box Diagram

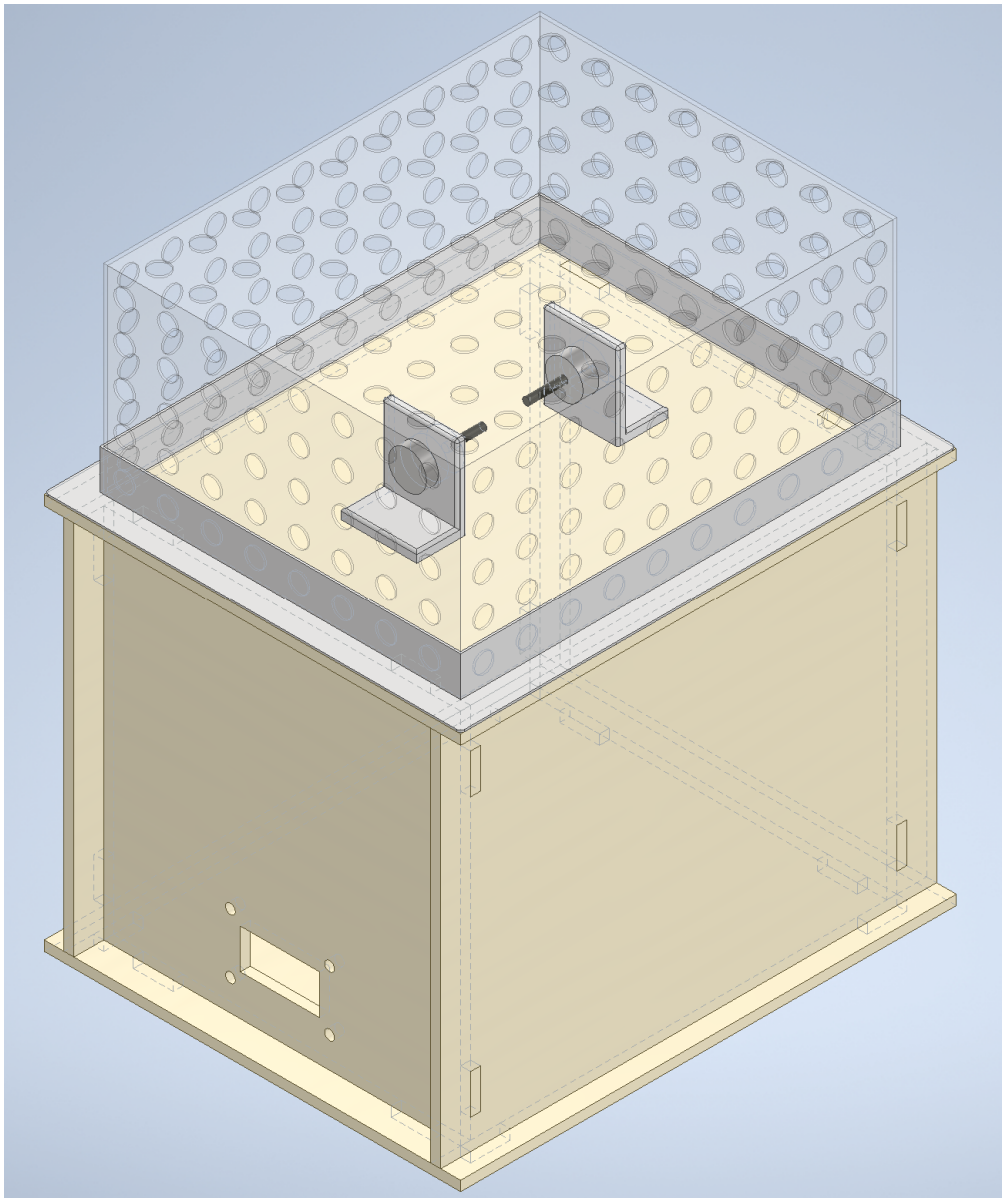


Figure 4.6.2: CAD Model

The enclosure design is one lower box to contain the electronics, and an upper section where the electrodes are contained within a perforated plexiglass box.

The bottom box will be made out of 5mm thick laser-cut treated plywood and fastened together using simple tongue and groove style joints. The following figures show the drawings for the 6 sides of the bottom box. Note that all dimensions shown are in millimeters.

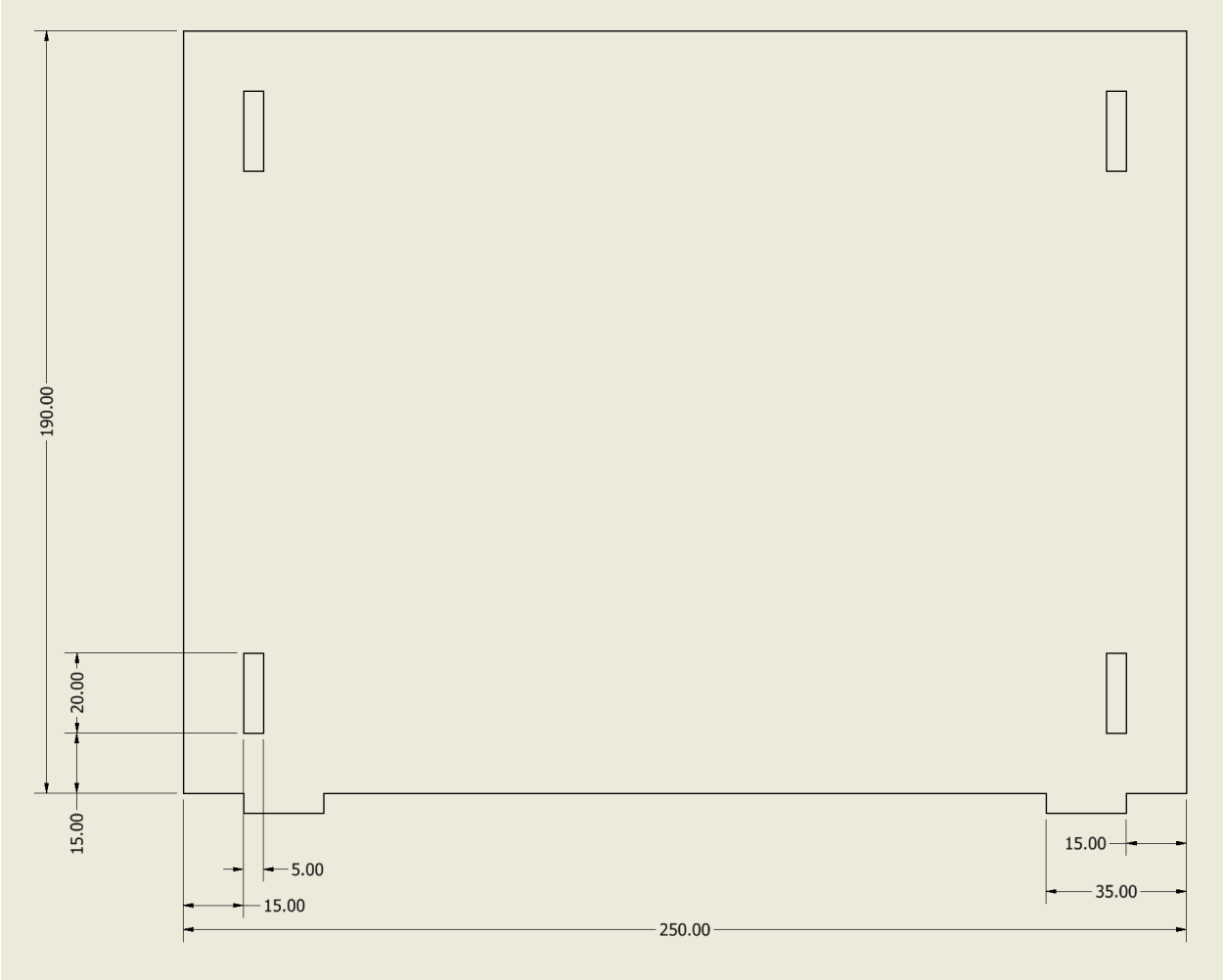


Figure 4.6.3: Lower Box Side 1&2

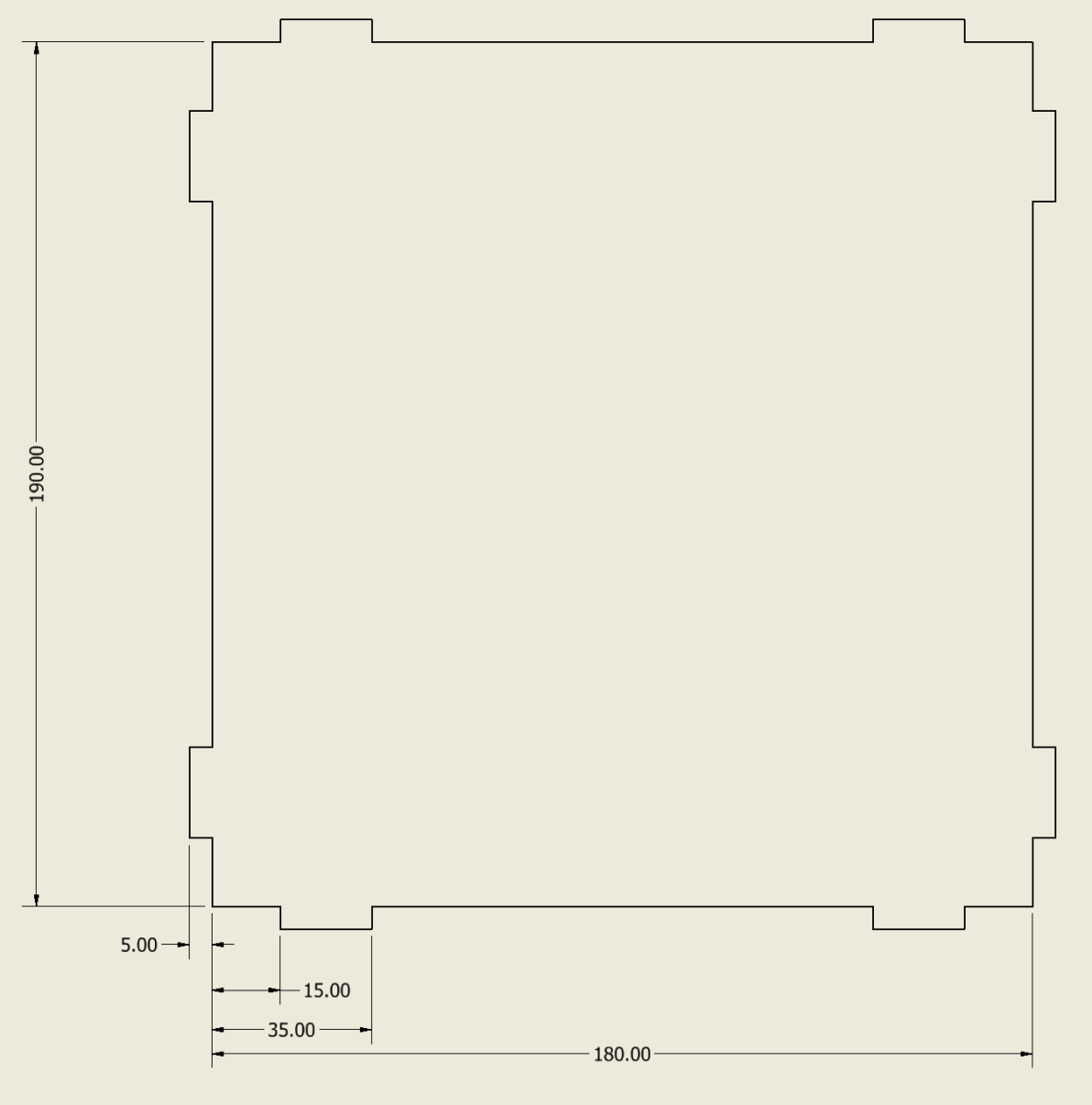


Figure 4.6.4: Lower Box Side 3

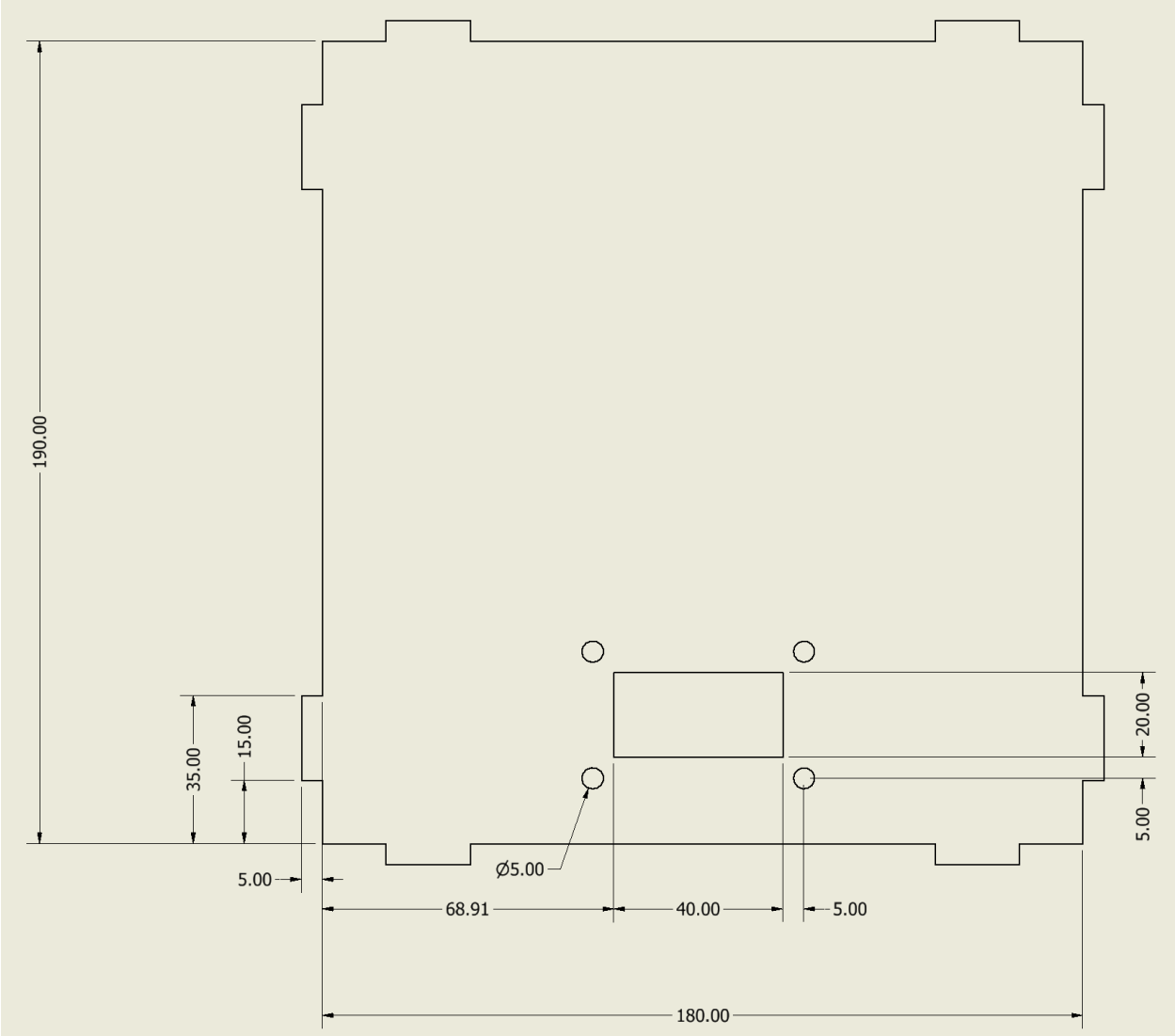


Figure 4.6.5: Lower Box Side 5

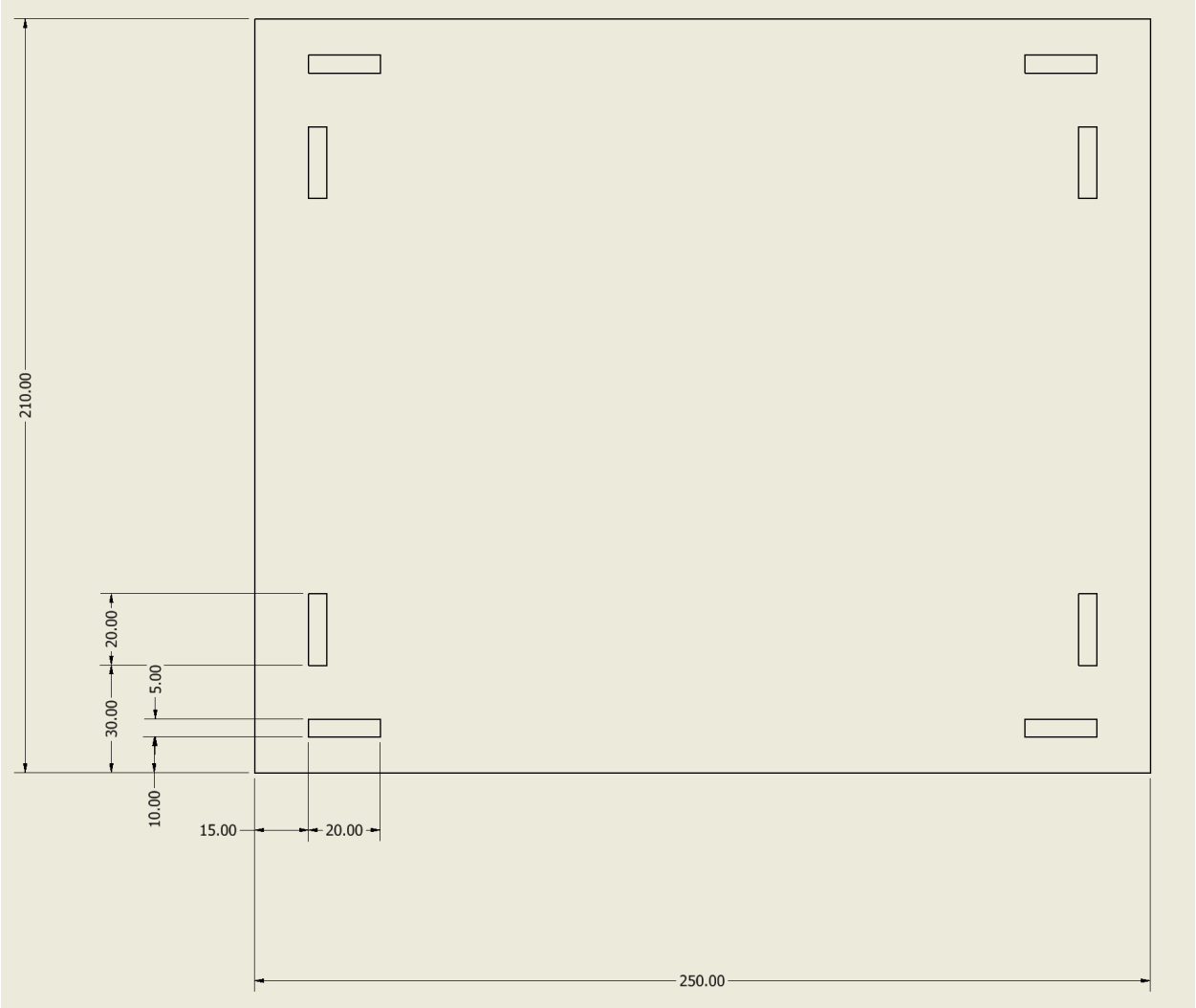


Figure 4.6.6: Lower Box Base

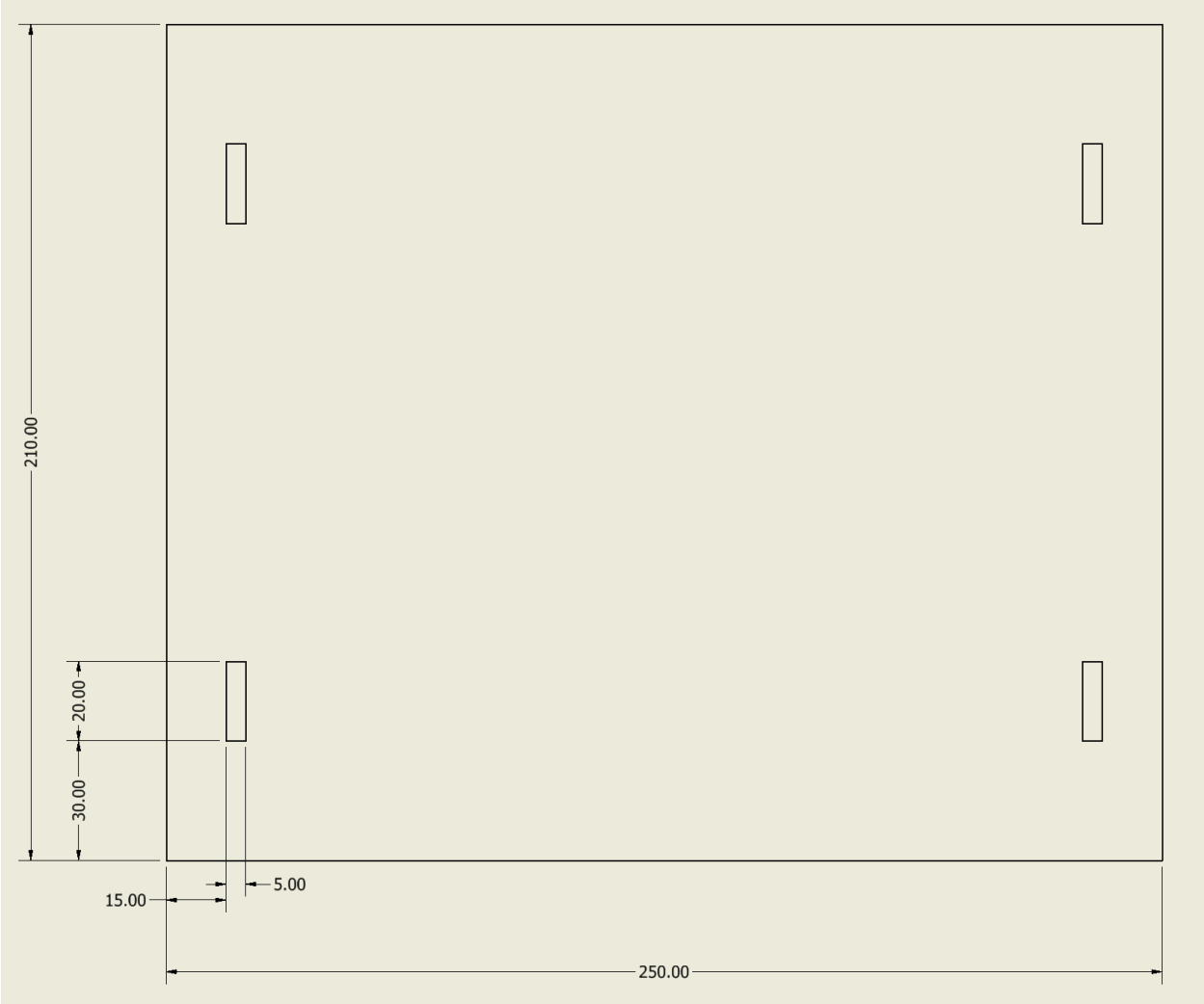


Figure 4.6.7: Lower Box Top

The tongue and groove style joints provide simple assembly/disassembly and will be glued (except for the top) once the system design is complete. The plywood construction also allows for the mounting points for the various blocks to change. Holes for mounting the subsystems will be drilled when they are completed and 3mm nuts/bolts with standoffs will be used for mounting each necessary component.

Side 5 of the lower box displayed in figure 5 has a mounting hole for the system's power input and shutoff switch. This mounting pattern is as per the component's drawings and 5mm diameter nuts and bolts will be used to fasten it to the enclosure.

The second part of the design is the top plexiglass box that allows for the display of the electrodes. This aspect of the design is necessary to prevent users from being able to touch the hot electrodes. The box will be made from 3mm laser cut clear acrylic. The dimensions in millimeters are shown in figure 8 below.

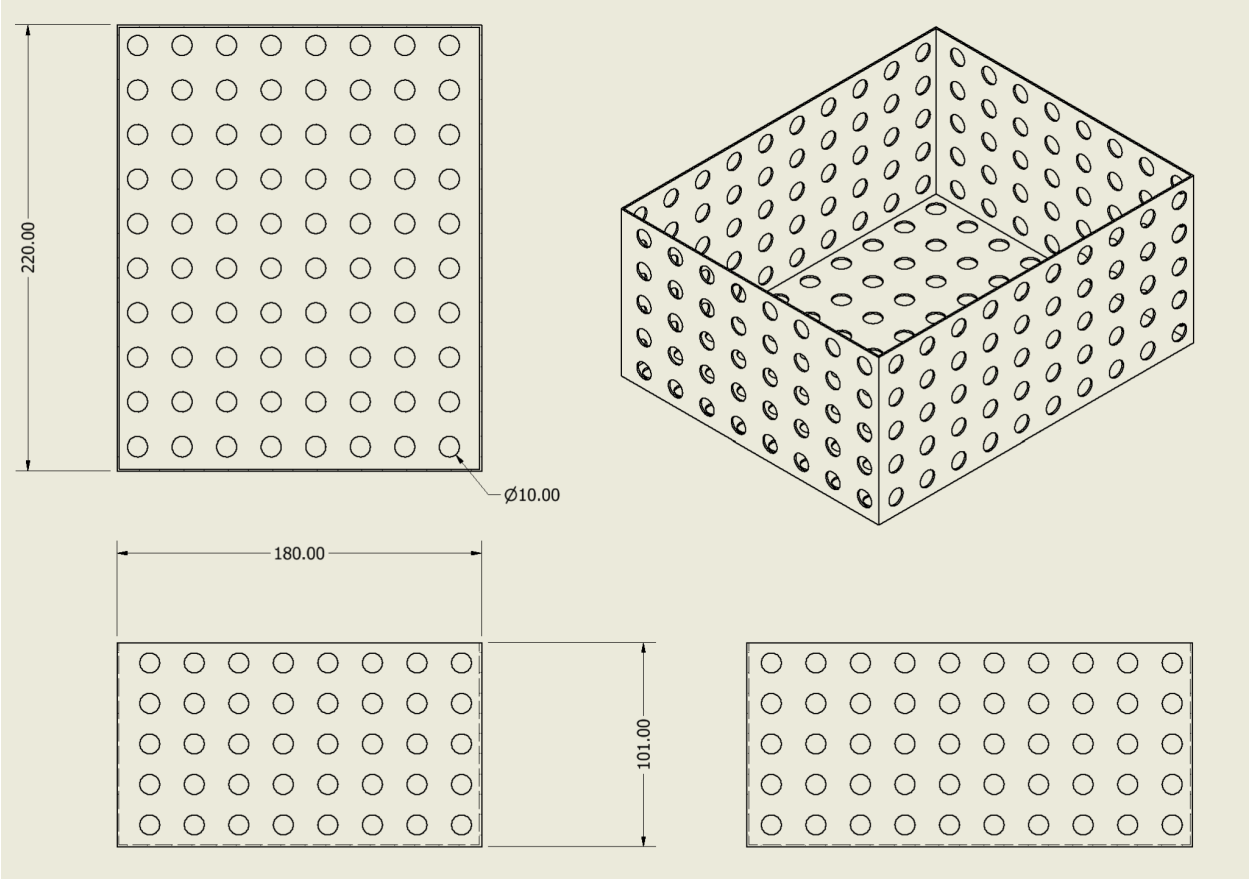


Figure 4.6.8: Acrylic Top Box

This box will be created from 5 separate sheets of acrylic and will be glued together as the piece will only need to be removed as one. The box also contains many perforations in the form of 10mm diameter holes cut into the acrylic. This is to best allow the sound from the electrodes to escape the box.

This will be mounted to the top of the lower plywood box via a 3D printed ABS frame fastened by screws. The drawings of that part are shown in figure 9 below.

The electrodes will be mounted to the top panel of the plywood bottom box, and contained within the top acrylic box. The electrode mounting system is yet to be designed, but the enclosure design shown above accommodates many possibilities as the mounting holes will simply be drilled as necessary. The CAD mockup of the design shown in figure 2 shows the electrodes mounted 0.75 inches above the base.

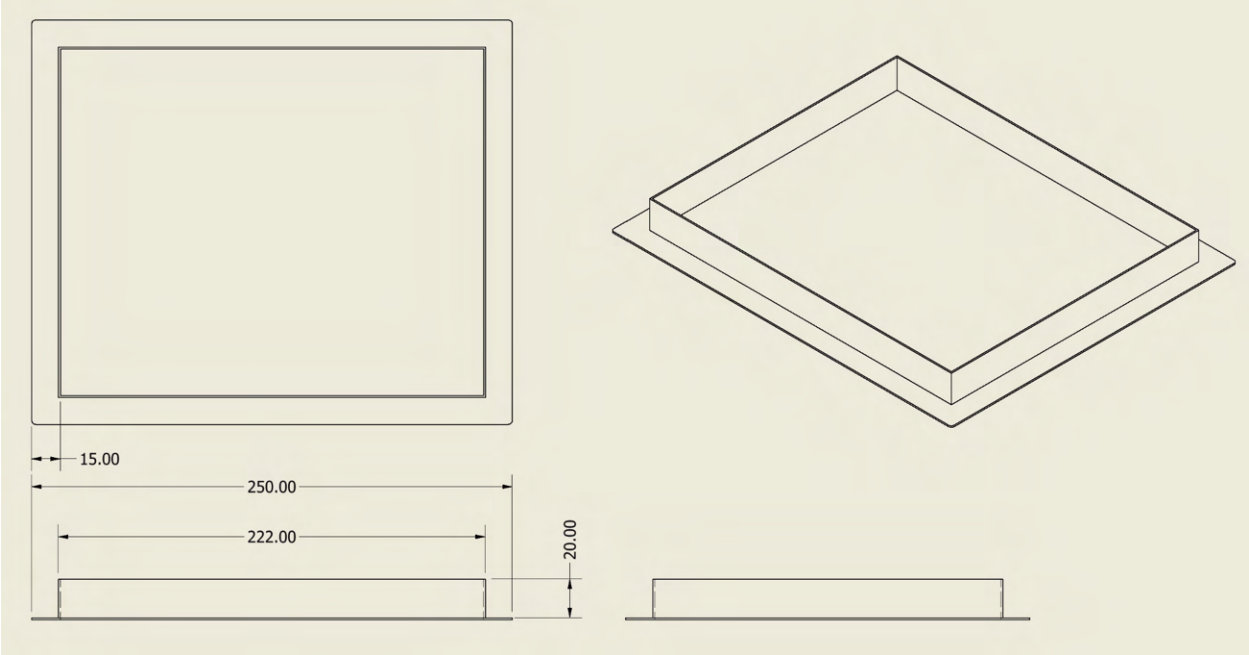


Figure 4.6.9: Acrylic Box Mount

4.6.3 General Validation

This enclosure design meets all of the system requirements for the block. Firstly, all of the speaker's subsystems fit within the enclosure. This is modeled in CAD below in figure 10. The CAD mockup includes correctly dimensioned models of the power system (bottom), transformer, FPGA board (blue), high power switching board (green), and the bluetooth receiver board (small, black). All of these components fit within the enclosure with plenty of room for wiring and adjustments. The finalized locations of the subsystems will be determined as their designs progress, and they will be mounted to the plywood enclosure via holes drilled and 3mm diameter bolts with nuts. Standoffs will be used as needed. This method allows for the placement of the components to be decided after their designs are fully completed, minimizing the risk of redesign of the enclosure.

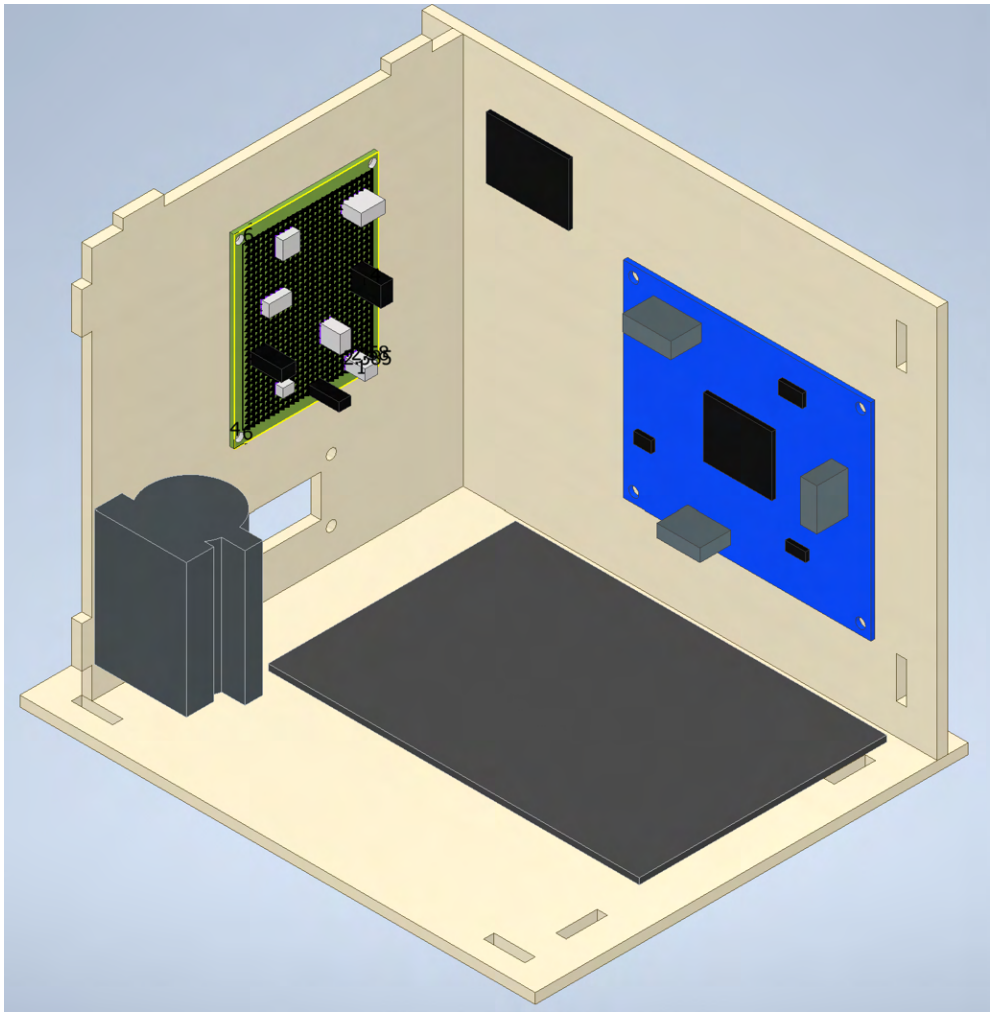


Figure 4.6.10: System Mockup

The material for both the top and bottom boxes of the enclosure is readily available at Tekbots where the laser cutting will be done. This means that re-fabricating any necessary parts will be simple and quick.

The 5mm thick plywood used for the bottom box to enclose the electronics is also a very good material to use for electrical safety. C. Skaar states in his well respected textbook that the approximate resistivity of plywood is 10^8 Ohms/cm for a high frequency AC signal [1]. Thus even if there was a catastrophic failure in the system and a high voltage was shorted to the enclosure, the insulation properties of the plywood would still ensure safety.

The top acrylic enclosure is necessary for safety precautions with the high voltage arcing electrodes. The design above results in the closest that a user could be to the electrodes as 85mm, exceeding the project's 4 inch requirement. This is assuming that the electrodes are mounted 0.75 inches above the top of the plywood box, and that a user is not sticking their fingers into the perforations in the acrylic box.

The nature of the clear acrylic means that the user of the speaker will also be able to clearly see the electrical arc at all times, thus fulfilling that requirement. One of the more notable design choices of the top acrylic box is the perforations. They are present to allow the audio from the electrodes to most efficiently spread outside of the speaker. Research was done concluding that a fully perforated box would create the highest fidelity audio vs just a few holes or a different hole pattern. This is because the holes allow the sound waves to escape the box somewhat evenly, and perforations on all sides reduces echo that causes distortion.

4.6.4 Interface Validation

No interfaces for the enclosure block.

4.6.5 Verification Process

1. Place component mock-ups in the enclosure using corresponding mounting points.
2. Ensure that each component and subsystem fits within the enclosure. If so, this verifies the enclosure.

4.6.6 References and File Links

[1] C. Skaar, “Electrical properties of wood,” *Wood-Water Relations*, pp. 207–262, 1988.

CAD Design Files - link

4.6.7 Revisions Table

Date	Topic	Revision
02/18/2022	Section 5 - Verification Plan	Verification plan added to test each property of each interface. Made instructions more clear based on feedback from Orian Hollar.
02/18/2022	References and File links	Added reference in IEEE format and added links to the CAD design files
02/18/2022	Section 4 - Interface Validation	Added descriptions for each interface property
02/18/2022	Section 3 - General Validation	Added general validation explaining why the design fulfills system requirements.
02/12/2022	Section 2 - Design	Added design details to the document including mechanical drawings, CAD drawings, and other design information
02/12/2022	Section 1 - Description	Added general size details to description via suggestion from Sam Wagner

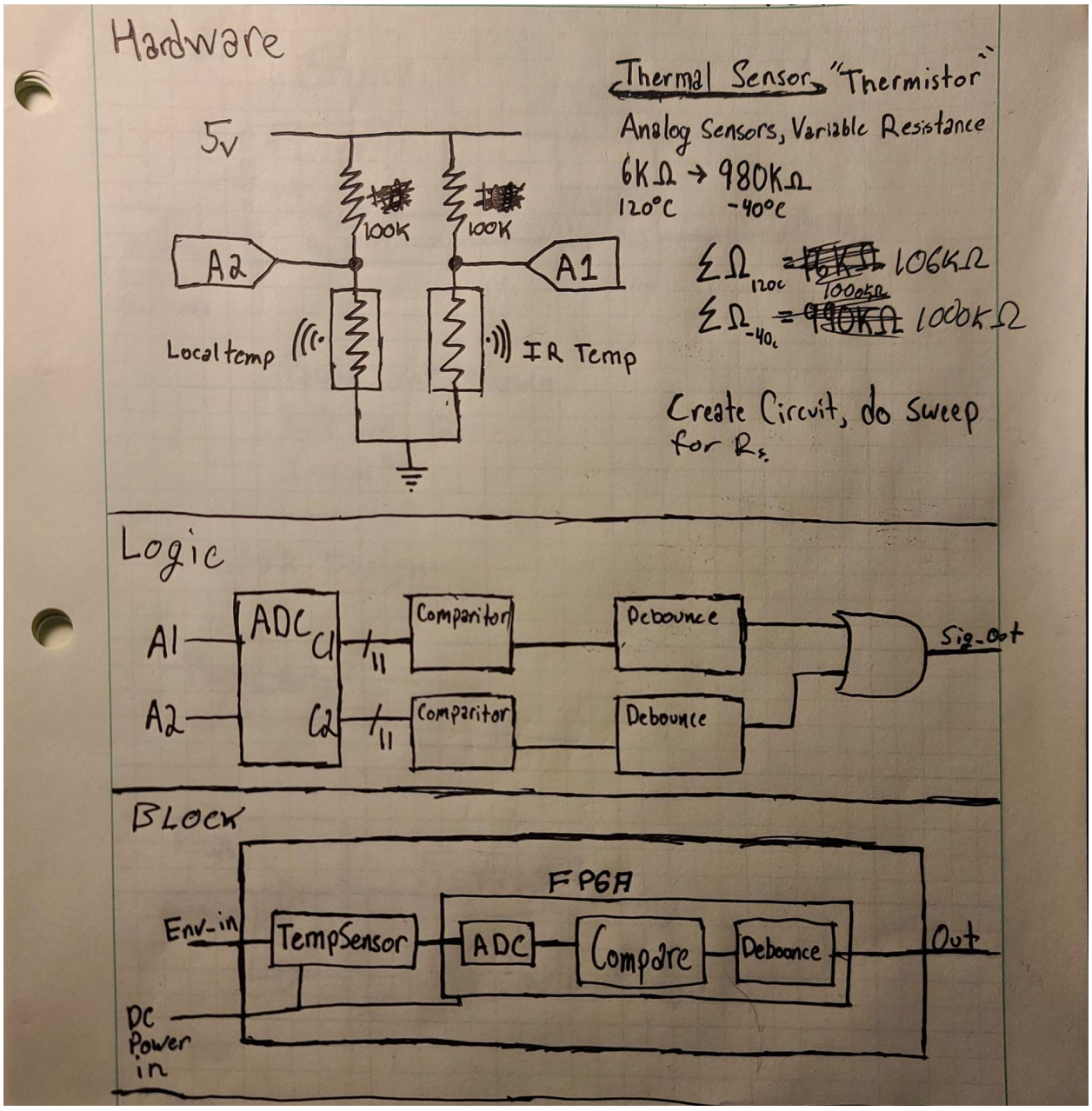
02/10/2022	Interface Updates	Mechanical mounting interface definitions were added for each necessary block
02/04/2022	Initial Draft	Initial Draft created by Kyle Barton

4.7 Safety Sensor

4.7.1 Description

This block is to ensure our system is safe to use for ourselves and users other than ourselves. Our team's safety system will have an emergency cutoff switch for an outside user to press at any time of the system's operation. This block will be directly connected to the power block so that the main power can be shut off at any point. This block will also be responsible for monitoring the system’s sensors and delivering digital control to all necessary components. This block will also be responsible for triggering fault signals based on sensor data. Another function of the Safety system is to put the speaker into an ‘idle mode’ when no audio input is detected by the Bluetooth receiver block. All of this logical functionality will be implemented on the system’s FPGA.

4.7.2 Design



4.7.3 General Validation

Our primary concern for safety is our enclosure or components overheating, so by getting a simple thermal sensor package to monitor the ambient temperature inside the enclosure and the absolute temperature of some vital components, this is possible. We already have the FPGA tested and have proved the use of the ADC. The simple voltage ladder is cost effective, small, and scalable. This block has been implemented and functions properly using a hot air gun to heat discarded ICs or the local sensor.

4.7.4 Interface Validation

Interface Property	Why is this interface this value?	Why do you know that your design details <u>for this block</u> above meet or exceed each property?
otsd_sfty_snsrs_systms_envin : Input		
Temperature (Absolute): 100 Celsius (IR temp)	It is the highest temperature our systems components are rated for, and should be measured.	Tested it in the lab!
Temperature (Absolute): 100 Celsius (Air/sensor temp)	Expected change in temperature within enclosure without heatsink ventilation, team's decided warning temperature.	Tested it in the lab!
Water: No water. 0CFS, no immersion.	Clarifying environment of sensor.	Tested in the lab.
sfty_snsrs_systms_pwr_asig : Output		
Other: Active High	Our FPGA's standard IO voltage. [1]	Tested it in the lab!
Vmax: 3.5 Volts	Our FPGA's standard IO voltage range. [1]	Tested in the lab. Pretty accurate.
Vrange: 0 - 3.5 Volts	Our FPGA's standard IO voltage range. [1]	Tested in the lab.

4.7.5 Verification Process

1. Use digital multimeter to show output voltage of asig
2. Heat test plate with air gun, monitor temperature on fpga/external thermometer.

4.7.6 References and File Links

[1] Terasic Inc., DE10-Lite User Manual. Available from: https://www.intel.com/content/dam/www/programmable/us/en/portal/dsn/42/doc-us-dsnbk-42-2912030810549-de10-lite-user-manual.pdf

4.7.7 Revisions Table

Date	Topic	Revision
03/6/2022		Verification plan added to test each property of each interface. Made instructions more clear based on feedback from Orian Hollar.

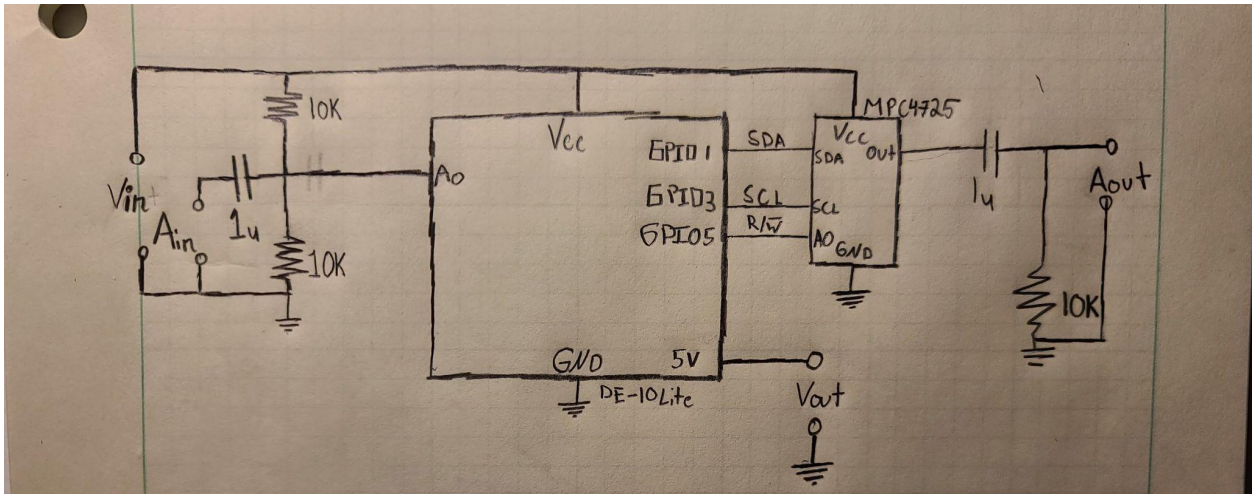
4.8 Signal Processing & Reconstruction

4.8.1 Description

As plasma speakers typically have significant distortion due to unstable diaphragm and airflow, it is beneficial to perform signal processing on the input audio to improve audio quality. There are four critical components: Sampling, Processing, Reconstruction, and Biasing. The bluetooth receiver block outputs a signal alternating at ±1V, so that alteration is biased around 2.5V to be within the range of the Analog to Digital Converter(ADC). The ADC is onboard the Field Programmable Gate Array (FPGA) development kit used for signal processing. A Digital to Analog Converter (DAC) capable of the same depth is used to reconstruct the output signal, which is then biased back around 0V. The system also passes power through to the Bluetooth receiver module through the regulator on the FPGA board.

4.8.2 Design

As seen in the black box diagram, the sub-system has two inputs and outputs each. One DC power input from the power sub-system and one analog audio input from the bluetooth represented on the wiring diagram below as Vin and Ain respectively. The outputs are analog audio and power for the bluetooth block, represented as Aout and Vout respectively on the diagram below.

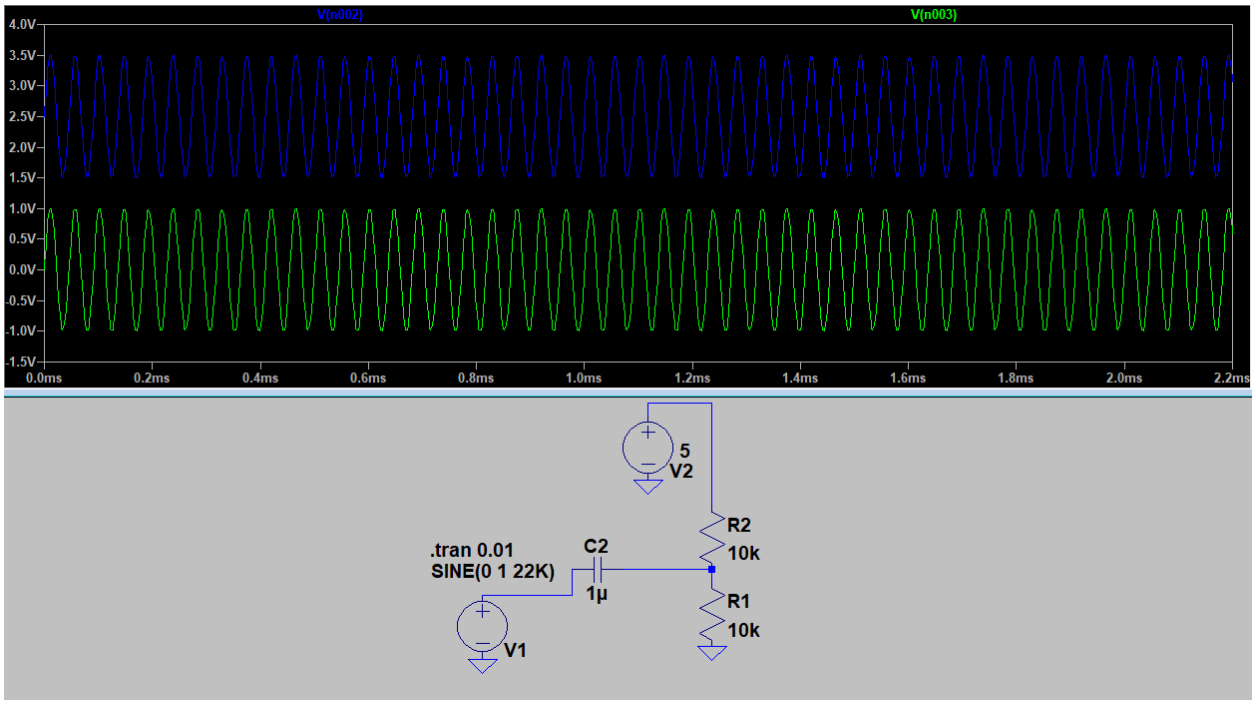


Wiring diagram

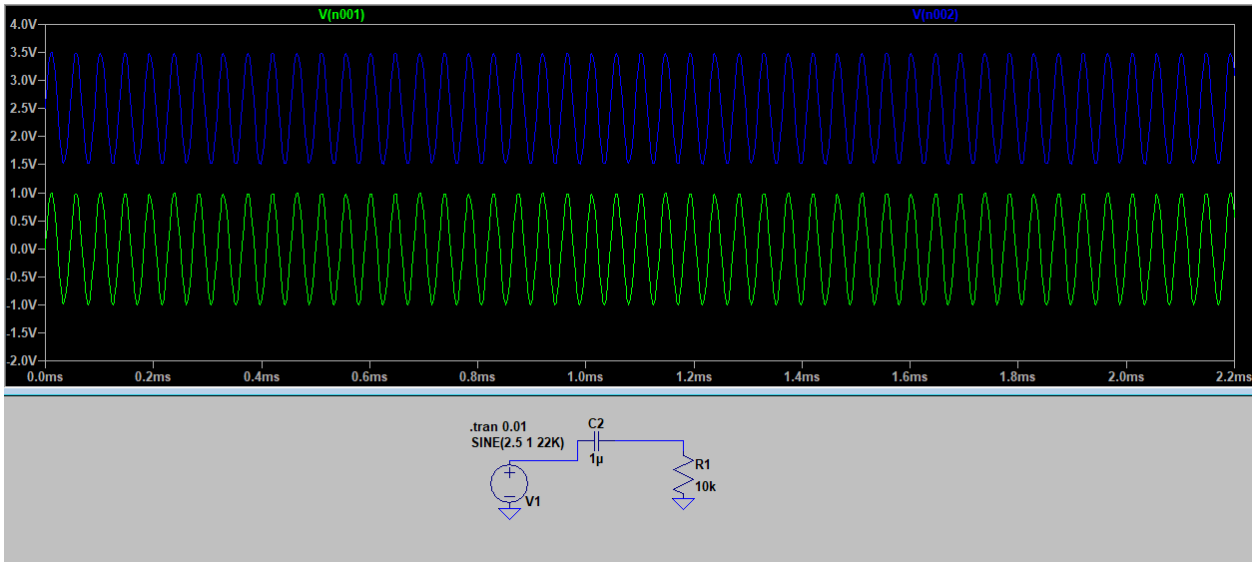
This diagram shows the entire hardware configuration of my block, with pin/silkscreen names and component values.

4.8.3 General Validation

The Biasing circuitry is easiest to validate with a simulation.



Input Bias Circuit. Blue signal is biased version of green



Output Bias Circuit. Green Signal is biased version of Blue.

According to their datasheets, the ADC can sample at a depth of 12 bits at 10MHz[1], and the DAC can output at a max of 3.4Mbps[2]. Thankfully sampling around a common audio rate of 44.1KHz yields an output datarate of 529.2Kbps sent to the DAC. This leaves plenty of space under the standard for address data.

To test the bluetooth receiver power I simply plugged it in. This interface is only in this block for ease of wiring. It worked!

4.8.4 Interface Validation

Interface Property	**Why is this interface this value?**	**Why do you know that your design details <u>for this block</u> above meet or exceed each property?**
pwr_sgnl_prcssng_rcnstrctn__dcpwr : Input		
Ipeak: 500m Amps	Max stated on DE10-lite User Manual.Spec is to handle sensor loads since they use the same board.[1]	System did not draw upwards of 30mA when tested.
Inominal: 150m Amps	Tested current drawn by DE-10Lite	Tested with 5V supply
Vmax: 5.5 Volts	stated on DE10-lite User	Tested with 5.5V supply

	Manual.[1]	
Vnominal: 5 Volts	stated on DE10-lite User Manual.[1]	Tested with 5V supply

sgnl_prcssng_rcnstrctn__wvfrm_gnrtn_mdltn_asig : Output

Max Frequency: 20K Hz	Common upper range of human hearing [3]	The DAC can output fast enough, the filters are tuned, and the FPGA is giant. Current logic takes less than 1% of available fabric. [2]
Vmax: 1.5V	Max output of DAC [2]	Tested, with 5V Vcc.
Vrange: +-1V	input range for IC used by WGM block.	The datasheet [2] says it'll go that high, and when I tested it, it did.

sgnl_prcssng_rcnstrctn__bltth_rcvr__dcpwr : Output

Inominal: 5m A	Tested draw	It was measured and was in range.
Vmax: 5 V	USB power avalible, just assumed	It worked.

bltth_rcvr__sgnl_prcssng_rcnstrctn__comm : Input

Max Frequency: 20K Hz	Common upper range of human hearing [3]	ADC can sample fast enough, and the bias simulation passes the frequency. [1]
Vmax: 1.5V	Has to be less than 2.5 for ADC, and this is what our chip was tested as outputting	The ADC can go up to 5v, with the 2.5 bias that's 4V. [1]
Vrange: +-1V	Standard range of loud music when tested.	With the bias it is in the range of the ADC. [1]

4.8.5 Verification Process

1. Show specifications of power supply, plug sub-system power in.
2. Connect phone to bluetooth receiver, open spotify, turn volume to max.
3. Connect Oscope probe to Bluetooth receiver output, AC coupling.
4. Demonstrate Negligible frequency components greater than 20KHz on input by adjusting time scale.

5. Demonstrate Vmax and Vrange on Oscope.
6. Disconnect Oscope probes, connect to Vout.
7. Connect Bluetooth receiver asig to sub-system.
8. Demonstrate Negligible frequency components greater than 20KHz on output by adjusting time scale.
9. Demonstrate Vmax and Vrange on Oscope.
10. Unplug sub-system power, replace power cable with split cable.
11. Attach DMM across split cable to measure current drawn.
12. Replace original power cable, replace bluetooth power cable with split cable.
13. Repeat Step #2. Attach DMM across split cable to measure current drawn.
14. Disconnect bluetooth power cable, Attach DMM to connection to measure Voltage.

4.8.6 References and File Links

[1] Terasic Inc., DE10-Lite User Manual. Available from: https://www.intel.com/content/dam/www/programmable/us/en/portal/dsn/42/doc-us-dsnbk-42-2912030810549-de10-lite-user-manual.pdf

[2] Microchip Technology, MPC4725 datasheet. Available from: http://ww1.microchip.com/downloads/en/devicedoc/22039d.pdf

[3] Purves D, Augustine GJ, Fitzpatrick D, et al., editors. Neuroscience. 2nd edition. Sunderland (MA): Sinauer Associates; 2001. The Audible Spectrum. Available from: https://www.ncbi.nlm.nih.gov/books/NBK10924/

4.8.7 Revisions Table

Date	Topic	Revision
1/20/2022	References	Reformatted References
1/21/2022	Verification Plan	Clarified terminology.

5. System Verification Evidence

5.1 Universal Constraints

5.1.1 The system may not include a breadboard

All of the electrical subsystems are constructed such that no breadboards are used. Description in the table below and photographic proof in figure 5.1 below:

Block	Construction
Enclosure	No electronics, no breadboard
High Power Switching	Student designed PCB and discrete components, no breadboard
Safety and Sensors	Discrete component and FPGA code, no breadboard
Signal Processing and Reconstruction	Off the shelf FPGA development board, no breadboard
Plasma Generation	Single transformer, no breadboard
Power	Off the shelf modules, no breadboard
Bluetooth Receiver	Off the shelf module, no breadboard
Waveform Generation and Modulation	Off the shelf FPGA development board, no breadboard

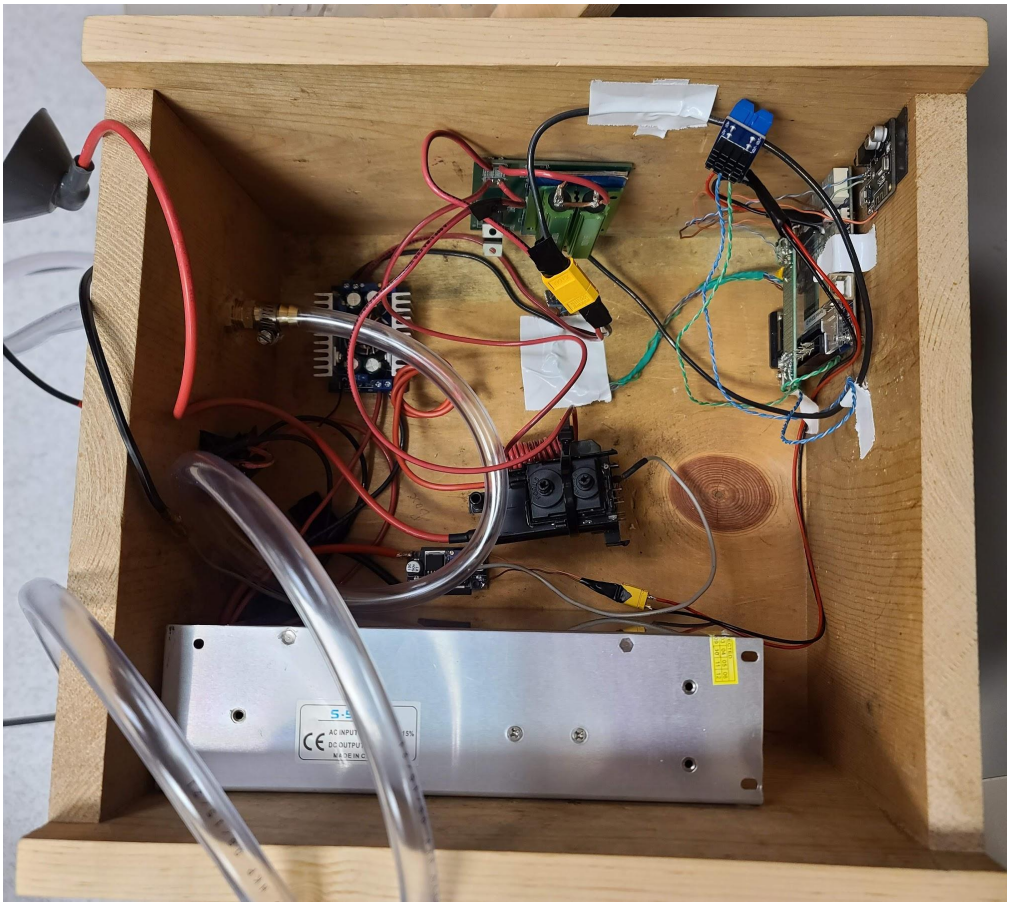


Figure 5.1: Full System Without any Breadboards

5.1.2 The final system must contain both of the following: a student designed PCB and a custom Android/PC/Cloud application*

Overall our team designed two PCBs.
The large PCB shown in figure 5.2 below incorporates transistors for the High Power Switching block, Inverting and Non-inverting Gate drivers for Waveform Generation and Modulation, and additional components required for Plasma Generation.

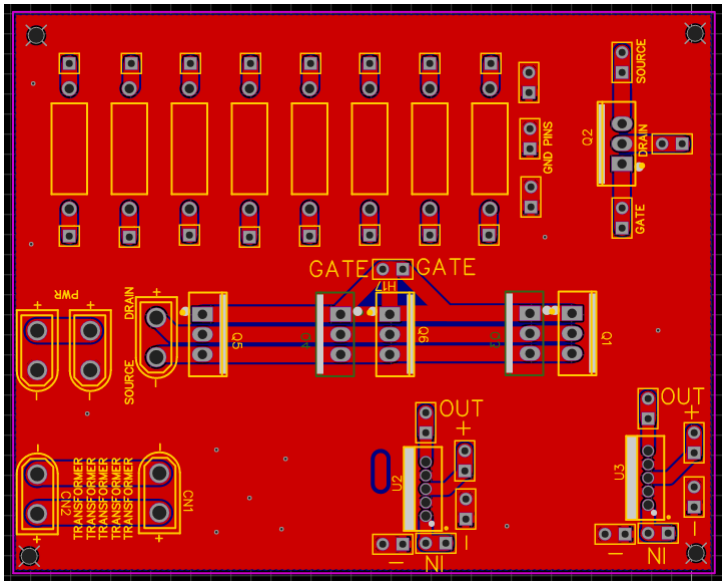


Figure 5.2: PCB #1

The smaller PCB is used for connections to the Safety Sensors block and shown in figure 5.3 below:

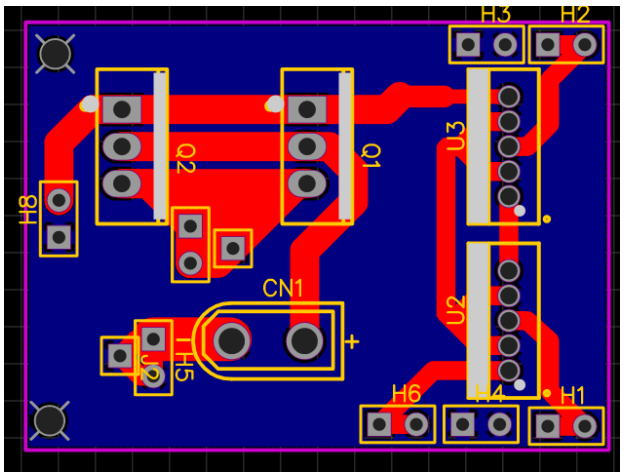


Figure 5.3: PCB #2

Android/PC/Cloud application requirement waived via Don in an in person meeting.

5.1.3 If an enclosure is present, the contents must be ruggedly enclosed/mounted as evaluated by the course instructor

All modules within the enclosure are either screwed into place, or secured with heavy-duty double sided tape. Simple shake test video to show that components will not shift while being transported - link.

5.1.4 If present, all wire connections to PCBs and going through an enclosure (entering or leaving) must use connectors

The only electrical connection going through the enclosure is the system main power. This power comes from a NEMA 15-5P AC power cable, plugged into a female socket mounted directly on the enclosure. This is shown in figure 5.4 below:

Figure 5.4: NEMA 15-5P AC Socket and Fused Switch

The helium gas line also passes through the enclosure via a brass fitting. This is shown in figure 5.5 below:

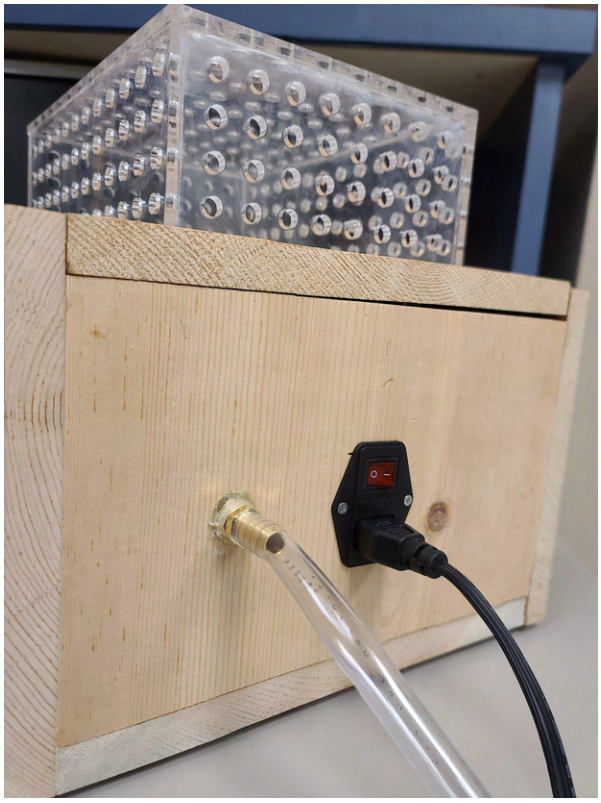


Figure 5.5: Helium Gas Line Through Enclosure

All connections to boards were made with Screw Gates or directional connectors.

5.1.5 All power supplies in the system must be at least 65% efficient

AC-DC Converter:
Measuring the AC power input is very difficult without the necessary equipment (power analyzer). Only the apparent power (in Volt-Amps) can be calculated with a digital multimeter by measuring the Vrms and Irms. The reactive power is not taken into account, and thus is likely a large overestimate of the true power. See figure 5.6 below [1]. Thus the efficiency for the AC-DC power converter was gathered from the datasheet linked here (see S-500-12 efficiency). The efficiency claimed on the datasheet is 84%, well above the 65% requirement. Thus even at all operating conditions it is safe to assume that the AC-DC converter is running above 65% efficiency.

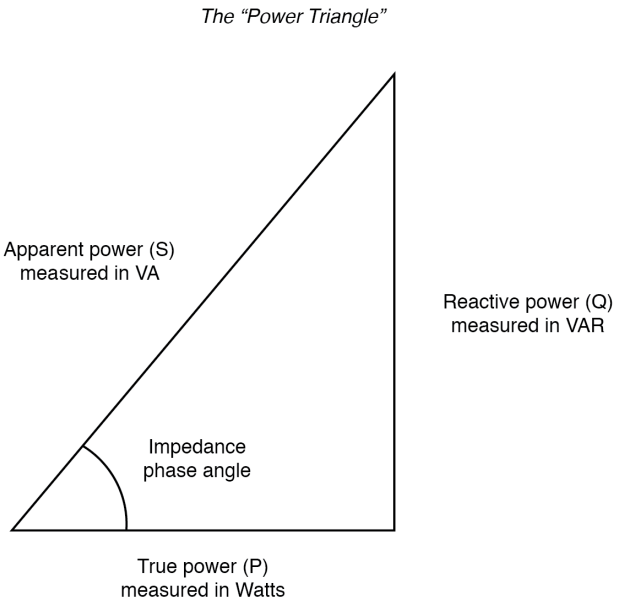


Figure 5.6: AC Power Triangle

30V Boost Converter: 88% efficiency

Tested Efficiency:
Pin = (12V)(0.372A) = 4.460W
Pout = (20.05V)(0.196A) = 3.9298W
Eff. = (3.9298)/(4.460)*100 = 88%

Video - Link

5V Buck Step Down Converter: 71% efficiency

Tested Efficiency:
Pin = (12V)(0.071A) = 0.852W
Pout = (5.00V)(0.121A) = 0.605W
Eff. = (0.605)/(0.852)*100 = 71%

Video - Link

5.1.6 The system may be no more than 50% built from purchased modules

Block	Construction
Enclosure	Custom Built
High Power Switching	Custom Built
Safety and Sensors	Custom Built
Signal Processing and Reconstruction	Custom Built
Plasma Generation	Custom Built
Power	Custom Built
Bluetooth Receiver	Purchased
Waveform Generation and Modulation	Custom Built

Out of the eight blocks, only the bluetooth receiver was purchased off the shelf, thus only 12.5% of the system is purchased modules.

5.2 The system is contained in a safe enclosure

5.2.1 Requirement

The system's enclosure shall not allow users to come within 2 inches of the electrodes.

5.2.2 Testing Process

1. Place electrodes within enclosure as they will be for final system
2. Insert measuring device through enclosure from the center of each of the 5 sides
3. Measure from each side the distance between the environment (outside the enclosure) to the closest part of an electrode
4. Ensure that all measurements give a minimum of 2 inches from electrode to environment

5.2.3 Testing Evidence

Video - link

5.3 The system is Bluetooth capable

5.3.1 Requirement

The system shall be able to input audio transmitted from a Bluetooth source.

5.3.2 Testing Process

1. Power on the system and start helium flow.
2. Using a Bluetooth 4.0 compatible audio transmission device, investigate the Bluetooth connection menu.
    a. This will be different depending on the outside device used.
    b. The outside device must have its bluetooth mode active, and be set to “scan” or “search” for new devices.
3. Locate a device called “BT5.0 Audio”
4. Attempt to connect to the device via Bluetooth
5. Verify the connection is made and the system is recognized as an audio output.
6. Play some audio at full volume.
7. Verify arc speaker activates

5.3.3 Testing Evidence

Bluetooth capable - link

5.4 The system is reliable

5.4.1 Requirement

The system will be able to play music for 60 seconds without overheating

5.4.2 Testing Process

1. Power on System and start helium flow.
2. Start input audio from connected bluetooth device
3. Use stopwatch to time system
4. Enjoy music for a minute.

5.4.3 Testing Evidence

Reliable - link

5.5 The system uses helium to produce an arc

5.5.1 Requirement

The system shall produce its arc in the presence of helium gas.

5.5.2 Testing Process

1. Power on the system and connect bluetooth.
2. Attempt to play music.
3. Verify that the system is unable to produce plasma.
4. Activate the flow of helium.
5. Verify the arc activates.

5.5.3 Testing Evidence

Helium - link

5.6 The system produces recognizable audio

5.6.1 Requirement

Audio recognition technology “Shazam” will be able to correctly identify the source audio.

5.6.2 Testing Process

1. Power on the system and connect a bluetooth capable device that will play music.
2. Position another device with music recognition software “Shazam” near the enclosure.
3. Play music through the bluetooth speaker.
4. Process the audio with Shazam.
5. Verify the recognised song is the same as the source.

5.6.3 Testing Evidence

Shazam - link

5.7 The system is responsive

5.7.1 Requirement

The system begins playing audio through the arc within 2 seconds of the music being un-paused.

5.7.2 Testing Process

1. Power on system, connect to bluetooth, and start the flow of helium gas
2. Verify arc is not active
3. Un-pause music and verify arc is activated and playing audio within 2 second time frame

5.7.3 Testing Evidence

Responsive - link

5.8 The system's arc is only active when music is playing

5.8.1 Requirement

System's electrical arc shall shut off within 2 seconds of the input audio signal being paused, and remain off until the audio signal is resumed.

5.8.2 Testing Process

1. Power system on and begin playing sound through Bluetooth audio, verify electrical arc is active
2. Pause audio
3. Verify that the electrical arc is no longer active within 2 seconds of pausing

5.8.3 Testing Evidence

Arc only active when music playing - link

5.9 Emergency shutoff switch

5.9.1 Requirement

The system shall have an emergency shutoff switch that powers off the arc in less than 1 second.

5.9.2 Testing Process

1. Power system on and activate the arc by playing music
2. Using a slow motion phone video camera, place a stopwatch within frame and begin recording and begin the stopwatch
3. Also within frame and with both the stopwatch and the speaker arc on, flip the emergency shutoff switch

4. Stop recording after 3 seconds. Verify in the slow motion video that the arc was disabled within 1 second of the emergency shutoff switch being flipped

5.9.3 Testing Evidence

Emergency shutoff: - link

5.10 References and File Links

[1] "True, reactive, and apparent power: Power factor: Electronics textbook," *All About Circuits*. [Online]. Available: https://www.allaboutcircuits.com/textbook/alternating-current/chpt-11/true-reactive-and-apparent-power/. [Accessed: 01-May-2022].

5.11 Revisions Table

Date	Topic	Revision
5/03/2022	Testing Evidence	Team: Added testing evidence video links for each requirement
5/01/2022	Universal Constraints	Team: Updated all of universal constraints evidence
5/01/2022	Power Supply Efficiency	Kyle: Added explanation for AC-DC power supply efficiency
4/22/2022	Section 5.2	Team: Completed testing plan for each requirement
4/20/2022	Section 5.1/ 5.2	Kyle and Jeffrey: Updated requirements section.
03/06/2022	Section 5.3	Ian: Updated section 5.3 to complete testing plan
03/06/2022	Section 5.2	Kyle: Updated section 5.2 to complete testing plan
03/03/2022	Initial Draft	Ian: Created initial draft of section 5

6. Project Closing

6.1 Future Recommendations

6.1.1 Technical Recommendations

1. Improved Switching Circuit

One major way that electronics within the speaker could be improved would be a re-design of the high-power switching circuit. This is the step that takes the lower-voltage PWM audio signal, and steps it up to a higher voltage and pulls (or pushes) it through the transformer. This circuit requires 20-40V and 2-6A to be switched relatively quickly at between 7-20kHz. Hence switching this much power is not an easy task.

Our final design used two MOSFETs in parallel to sink current through the transformer (transformer was *above* the MOSFETs in the circuit with the high side tied to Vdd and the low side tied to the drain of the MOSFETs). This layout worked, but still all of that power was getting switched through only two MOSFETs and they got very hot very quickly. To remedy this, we placed low-ohm power resistors in series with the transformer to limit the current. This solution also worked, but the resistors constantly burned power and made the system less efficient.

Likely the best solution for switching the high-power signal would be an H-bridge circuit powered by dedicated gate drivers. This H-bridge would also include the added benefit of switching the direction of current through the transformer, theoretically increasing the fidelity of the output audio. Dedicated gate drivers would supply higher voltage to the gates of the MOSFETs and would allow them to switch more efficiently, dissipating less power and thus less heat.
Another possible benefit of an H-bridge circuit would be that it would allow the high-power switching to occur at a higher voltage and thus create a louder speaker. Because of thermal and component limitations, our final speaker did not produce sound as loud as desired.

Since we ultimately switched around 20KHz, there was a large amount of “dead time” where the transformer was saturated. This is what necessitated the 200W 4Ohm Resistor to be placed in series with the transformer. If a much faster switching speed was used, and the transformer was stopped from basically shorting the switching block, then all the power lost by the resistors would be able to be used in the arc.

The thought process behind this and a more detailed analysis can be found in the IEEE article *Design and Evaluation of Electronic Circuit for Plasma Speaker* [1].

2. Filtering for the Arc

Another technical recommendation for this project's possible future would be to experiment with filtering on both the primary and secondary sides of the transformer. General noise and switching noise cause the waveform going into the transformer to not be far from the ideal PWM signal. The transformer then amplifies this noise and the final output signal over the electrodes is very dirty. High voltage spikes cause audible imperfections in the output sound.

Filtering the signals with passive components would smooth out this waveform and result in a more *natural* tone for the speaker. Passive components could also improve the switching of the circuitry and even further improve the sound quality of the output.

Some recommendations include snubbing circuitry on the input side of the transformer. Capacitors to ground and possibly zener diodes to suppress voltage spikes in the signal. Capacitors to ground would also reduce the general noise in the signal likely caused by the power supply. Although obvious, corner frequencies of the capacitors would have to be carefully considered to not affect the signal within the expected switching frequencies. Voltage ratings of the components would also have to be considered as they would be on a relatively high voltage signal. Similar filtering could also be done on the high-voltage output side of the transformer, but special high-voltage capacitors would need to be used.

Another similar filtering idea would be to experiment with "bypass" capacitors near the electrodes. Theoretically the capacitors could supply much quicker voltage to the electrodes, making the switching much cleaner. Again, very high-voltage capacitors would need to be used, and their charging time would need to be analyzed to ensure they would be effective.

3. Improved Helium Chamber

Since our decision to use helium was rather last minute, our helium chamber was made out of a powerade bottle with holes burned into it. The basic principle is to have the electrodes high up in a sealed portion of the chamber, where helium accumulates and saturates the area surrounding the electrodes. It still needs to be able to interact with the air outside the chamber, and ideally this will be a pathway with acoustic design.

4. Further Control of Arc

The last major technical recommendation for future project development would be to implement systems to have more control over the arc. Parameters such as arc distance and voltage have a major impact on the properties of the arc, and small changes seem to make a big difference. Our system was not designed to make these parameters easily tweakable, and thus we were unable to experiment and figure out the optimal conditions. If you were able to experiment with the arc parameters and find an optimal setup, it would likely result in a much better output sound.

One recommendation to achieve this would be to implement a mechanical system to adjust the distance between the electrodes. Possibly a rack and pinion style gear system with labeled markings every ~2mm. This way the designers could adjust the distance between the electrodes with a screw and fine tune the audio quality for different operating conditions.

Another recommendation on this subject would be to have the high power switching voltage be adjustable. This is fairly straightforward to achieve on a buck or buck-boost converter and could be done by an external potentiometer. Having this adjustment would again allow for fine tuning of the arc characteristics and audio quality. It could possibly also serve as a sort of volume control for the speaker, but this idea is untested.

6.1.2 Global Impact Recommendations

1. Explore Fire Speaker

6.1.3 Teamwork Recommendations

1. Better Communication on Progress

Our team struggled with teamwork throughout the project. Although this is expected, there are strategies to be implemented so that the teamwork problems do not affect the quality of the final design. One main recommendation for this would be to ensure very clear and open communication within the team on each member's progress with their work. Keeping a clear gauge on the team's technical progress will allow more proficient members to pick up the slack, and prevents scrambling to get work done last minute. Although the goal is to split the work evenly between the members, this is often unrealistic and can hinder a team.

Specifically, this communication on progress could be done through activity reports [3]. They would not need to be long or detailed, but a weekly activity report from each team member would highlight the progress completed along with the challenges and where the member fell short on their work. Then each team member would be aware of the progress and the team can decide a course of action for each necessary task.

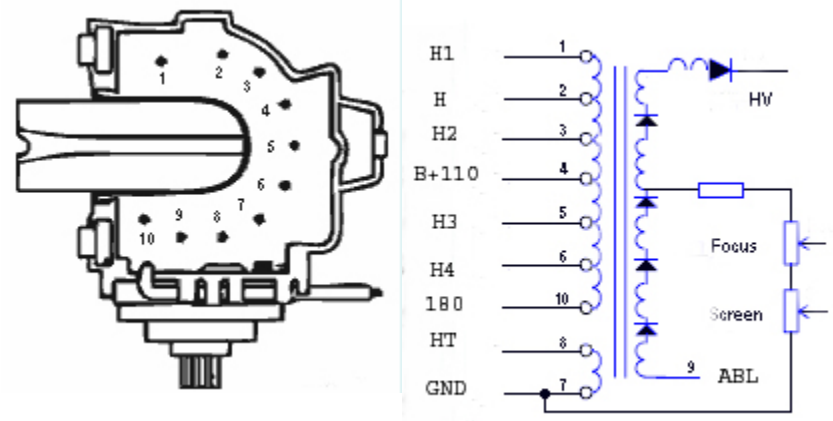
2. Quality of Work and Documentation Standards

Throughout the project, the quality of work produced by the team was often times embarrassingly bad. This caused many problems when integrating all the blocks of the system together near the end of the project. The work done prior was often lacking, just barely meeting expectations, and thus any small change to the original block would require a full redesign. If the initial designs of the block were truly modular and followed solid interface definitions this would have been avoided. In general it was difficult to convey what was expected, and a lack of solid project management and delegation led to some vastly different interpretations of what certain members were responsible for.

One solution to this problem would be to set up quality standards for the work and documentation done by each team member. Putting thought into this early in the project would save time in the long run, and there would be no question as to what is expected. A very thorough and professional example of this can be seen in the IEEE Standards for Software Documentation [4]. Although there is not a need for such a thorough process for a project this small, the same general idea and thought process can be applied to create similar standards for work quality and documentation quality.

6.2 Project Artifacts Summary

PCB Artifacts: Link
Bluetooth Board: Link
Enclosure CAD Files: Link
Power Artifacts: AC-DC power supply Datasheet - Link
Boost Converter - Link
Buck Converter - Link
FPGA Artifacts: Link
Flyback Transformer Pinout:



6.3 Presentation Materials

(links will be updated once completed)

Presentation Poster - Link
Virtual Showcase - Link
Expo Introduction Video - Link

6.4 References and File Links

[1] D. Severinsen and G. Sen Gupta, “Design and Evaluation of Electronic Circuit for Plasma Speaker,” *Proceedings of the World Congress on Engineering*, vol. II, Jul. 2013.

[2] B. A. Glowacki, W. J. Nuttall and R. H. Clarke, "Beyond the Helium Conundrum," in *IEEE Transactions on Applied Superconductivity*, vol. 23, no. 3, pp. 0500113-0500113, June 2013, Art no. 0500113, doi: 10.1109/TASC.2013.2244633.

[3] Purdue Writing Lab, “Activity Reports,” *Purdue Online Writing Lab*. [Online]. Available: https://owl.purdue.edu/owl/subject_specific_writing/professional_technical_writing/activity_and_postmortem_reports/activity_reports.html. [Accessed: 06-May-2022].

[4] V. Phoha, "A standard for software documentation," in Computer, vol. 30, no. 10, pp. 97-98, Oct. 1997, doi: 10.1109/2.625327.