Tachyon VNX FPGA Card

User Guide

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Table of Contents

Table of Figures

List of Tables

1. About this Document

This document is intended to provide an overview of the Tachyon VNX card. All major blocks are described so that users are able to utilize the card to its full capabilities. The user guide may be used as a reference for all the relevant hardware details of the card for engineers working with designs on the Tachyon.

1.1. Conventions

The nomenclature used in this document is based on the Verilog Language. This includes radix indications and logical operators.

1.1.1. Data Ordering and Data Types

Data ordering is as per the RapidIO specification. This includes:

- Byte ordering is big-endian
- The most significant bit within data types is numbered zero.

Table 1 Data Types

Name	Size
byte or octet	8-bits
hword – half word	16-bits
word	32-bits
dword – double word	64-bits

Note that in PCI Express specification a dword is used to denote a 32-bit quantity and a little-endian convention is used.

1.1.2. Signal Names

- Signal names may be in either case and typically follow the conventions of the interface with which they are associated.
- Signal names that end with “_n” or “_N” are active low.

2. Overview

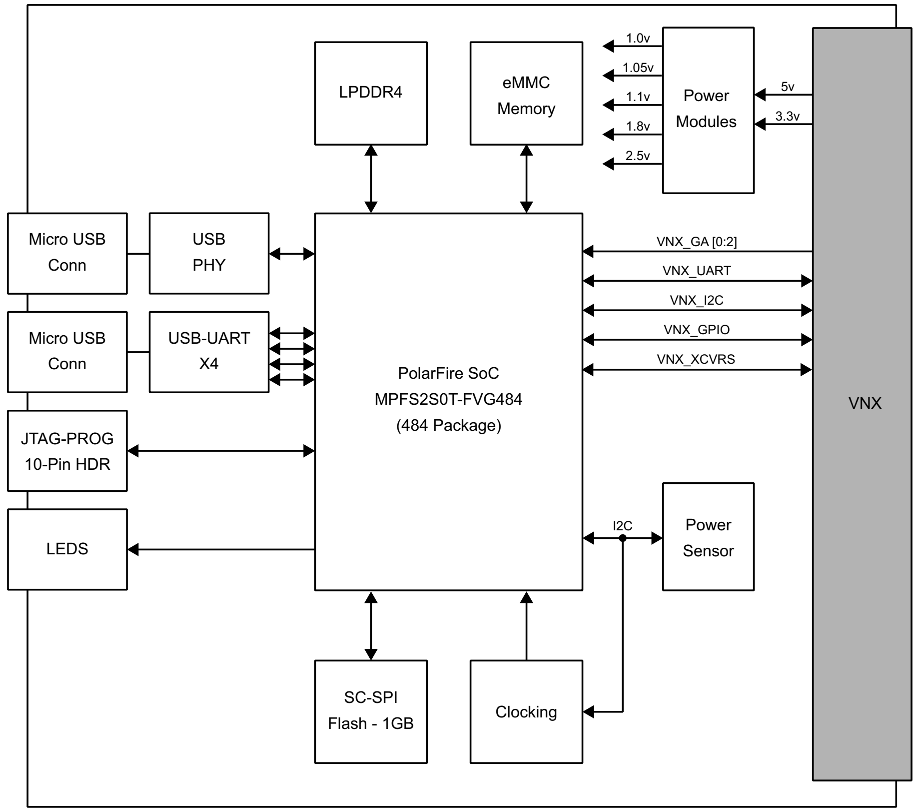
The Tachyon FPGA Card is a Space VNX form factor FPGA card utilizing a PolarFire SoC FPGA. The card is designed to support the following use models

- Prototyping: The card can be used to prototype IP designs on the PolarFire FPGA and test interoperability with other Space VPX cards.
- IP Evaluation: With four transceivers brought to the VNX connector, the card can be used to evaluate designs based around high speed serial interfaces.
- Education: The flexibility of the FPGA paired with high density I/O makes this card suitable for a variety of applications and educational opportunities.
- Processing: The PolarFire device supports a multi core 64-bit RISC-V processor subsystem. Paired with the FPGA fabric, the SoC is ideal for exploring embedded designs and tradeoffs between software and hardware solutions

The card supports the Microsemi PolarFire MPFS250T-FCVG484EES device.
Features of the card include

- 8 GB eMMC flash
- Micro USB 2.0 Hi-Speed OTG
- Four serial transceiver lanes
- External SPI flash memory for configuration images
- 400 pin count VNX connector
- 4 GB of ECC protected DDR4 SDRAM

Figure 1 Tachyon VNX FPGA Card Block Diagram



3. Clocking

The Tachyon board provides three clocking sources for the PolarFire SoC device:

- 50 MHz oscillator for general purpose clocking of the FPGA fabric
- 100 MHz transceiver reference clock from the VNX connector
- Programmable transceiver reference clock from an on-board clock generator

Table 2 provides a summary of the clocking resources.

Table 2 Clocking Resource Summary

Clock Name	Frequency	Clock Source
50MHZ_B0_1P8V	50 MHz	U_TBD DSC1001DL5-050.0000 oscillator
XCVR_0A_REFCLK	100 MHz	VNX backplane CLK0_P/N pair
XCVR_0B_REFCLK	Programmable	U_TBD Si570 programmable clock generator

3.1. 50 MHz Oscillator

A Microchip DSC1001DL5-050.0000 50-MHz clock oscillator with an accuracy of +/-10 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock. Other frequencies can be generated within the FPGA through the use of on-chip clocking resources.

Figure 2 shows the 50-MHz clock oscillator interface.

Figure 2 50-MHz Clock Oscillator Interface

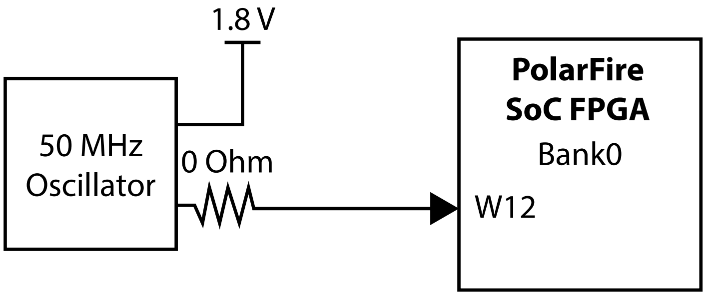


Table 3 50 MHz Clock Details

Clock Source Ref. Des. and Pin	Schematic Net Name	I/O Standard	FPGA (UTBD) Pin
UTBD.3	50MHZ_B0_1P8V	LVCMOS 1.8	W12

3.2. 100 MHz Transceiver Reference Clock

This transceiver reference clock is sourced from the CLK[0]_P/N pair on the VNX backplane connector. This clock is driven by the VNX System Controller at a rate of 100 MHz. This clock is also correlated (i.e. it has exactly the same frequency) as the 100 MHz reference supplied to other modules on the backplane. This means that clock compensation techniques are not required for serial connectivity between cards that use these clocks as their transceiver reference.

Figure 3 100 MHz Transceiver Reference Clock Interface

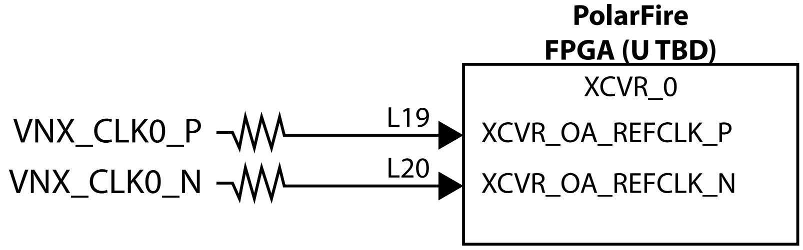


Table 4 100 MHz Transceiver Reference Clock Details

Clock Source Ref. Des. and Pin	Schematic Net Name	I/O Standard	FPGA (UTBD) Pin
UTBD.G15	VNX_CLK0_P	HCSL	L19
UTBD.G16	VNX_CLK0_N	HCSL	L20

3.3. Programmable Transceiver Reference Clock

This transceiver reference clock is sourced from an Si570 programmable clock generator. The default frequency for the clock is 156.25 MHz, but this can be changed by the MSS through the on-board I2C interface. The I2C interface address for the clock generator is TBD. For programming information for the Si570 device can be found in the Si570 datasheet.

Figure 4 Programmable Transceiver Reference Clock Interface

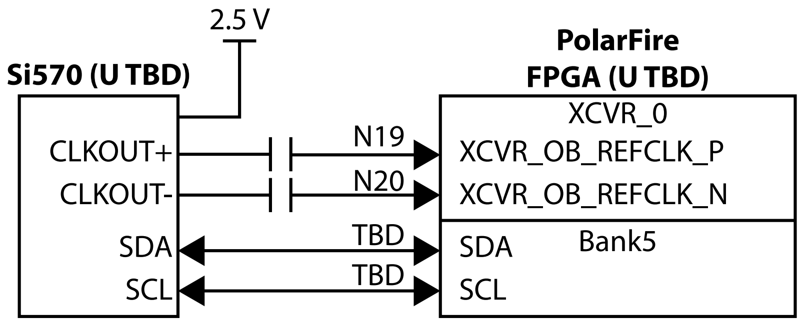


Table 5 Programmable Transceiver Reference Clock Details

Clock Source Ref. Des. and Pin	Schematic Net Name	I/O Standard	FPGA (UTBD) Pin
UTBD.TBD	PROG_CLK_P	LVDS	N19
UTBD.TBD	PROG_CLK_N	LVDS	N20

4. Power Supply

The Tachyon is powered via two feeds from the VNX connector. The VNX connector supplies a 5V and 3.3v power feed which is used to derive other voltages used by the card and power components. The voltage regulator currents are monitored by the PolarFire FPGA using a Microchip PAC1934T-I/JQ Power/Energy monitor. Figure 5 illustrates the power supply architecture and Table 4 describes the voltages and loads.

Figure 5 Power Supply Block Diagram

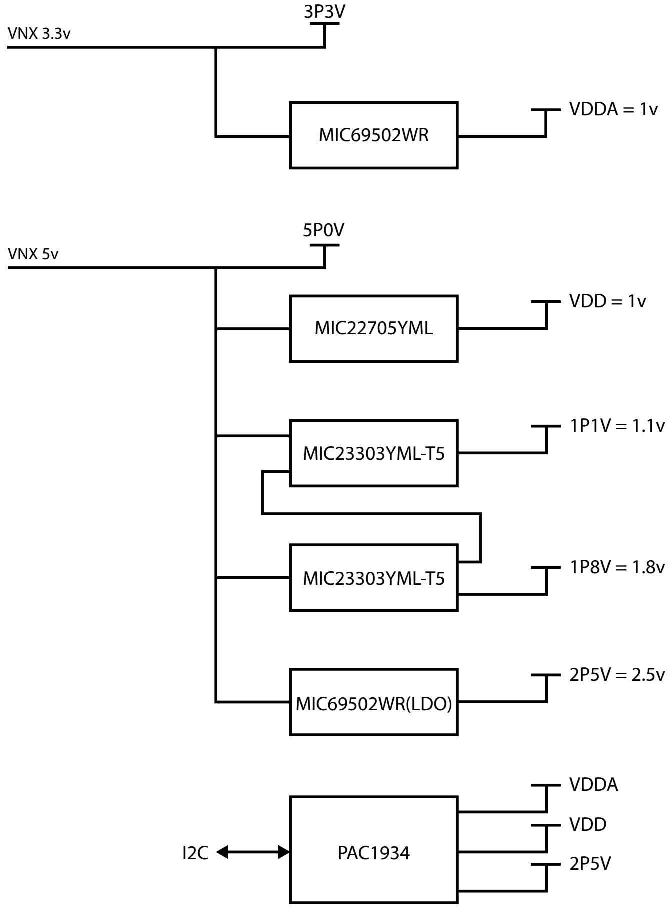


Table 6 Voltage Association and Load

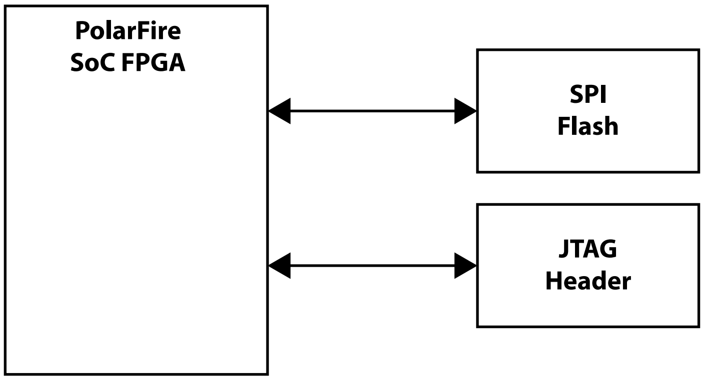
Voltage Supply	Voltage	Name	Load
VNX Connector	3.30V	3P3V	• MIC69502WR • eMMC • SC-SPI • JTAG • UART • 50MHz CLK • LEDs • PolarFire • Bank 1, 2, 3, 5 • Device Reset
MIC69502WR	1.00V	VDDA	SerDes Channel
VNX Connector	5.00V	5P0V	• MIC22705YML • MIC23303YML-T5 • MIC69502WR (LDO) • USB_PHY
MIC22705YML	1.00V	VDD	Core Power
MIC23303YML-T5	1.10V	1P1V	• PolarFire Bank 6 • LPDDR4
MIC23303YML-T5	1.80V	1P8V	• PolarFire Bank 0 • 50 MHz Clock • DDR4 Device Power
MIC69502WR(LDO)	2.50V	2P5V	VDD_XCVR_CLK

5. Device Configuration

The PolarFire SoC FPGA fabric can be programmed via JTAG or onboard SPI flash memory. The JTAG header, in conjunction with a FlashPro programmer, can be used to program the device from a host PC via Microsemi's FlashProExpres software. The JTAG header also allows user to debug designs using Microsemi's Smart Debug.

The Tachyon also supports 1 GB of SPI flash memory which can be used to store boot images for the FPGA, allowing the device to boot without any connection to a host PC.

Figure 6 Device Configuration High Level Block Diagram



5.1. SPI Serial Flash

The Tachyon has 1 Gb of SPI flash memory. The SoC uses SPI master programming mode as described in section 2.3.3 of Microsemi's UG0914 and is connected to Bank 3 of the device.

- Part number: MT25QL01GBBB8ESF-0SIT
- Manufacture: Micron

Figure 7 SPI Flash Interface

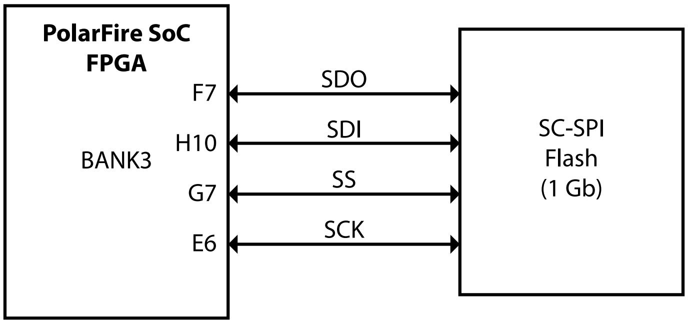


Table 7 SPI Pin Names and Descriptions

Net Name	Pin Number	Direction	I/O Standard	Description
SC_SPI_SCK	E6	Output	3.3V	Serial clock
SC_SPI_MOSI	F7	Output	3.3V	Master out slave in
SC_SPI_MISO	H10	Input	3.3V	Master in slave out
SC_SPI_SS	G7	Output	3.3V	Slave select

5.2. JTAG Interface

The JTAG interface is used for device configuration and on chip debug. The JTAG pins interface to the user's PC via an external FlashPro6 device over USB. The JTAG interface is connected to Bank 3 of the SoC.

Figure 8 JTAG Programming

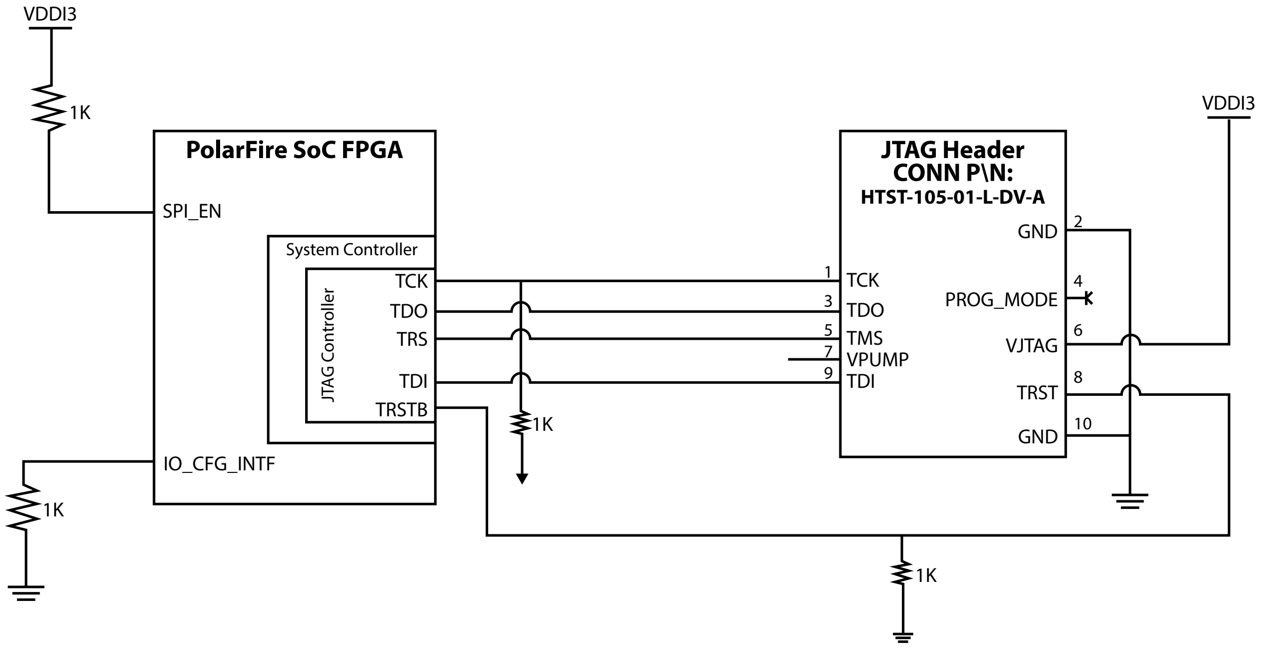


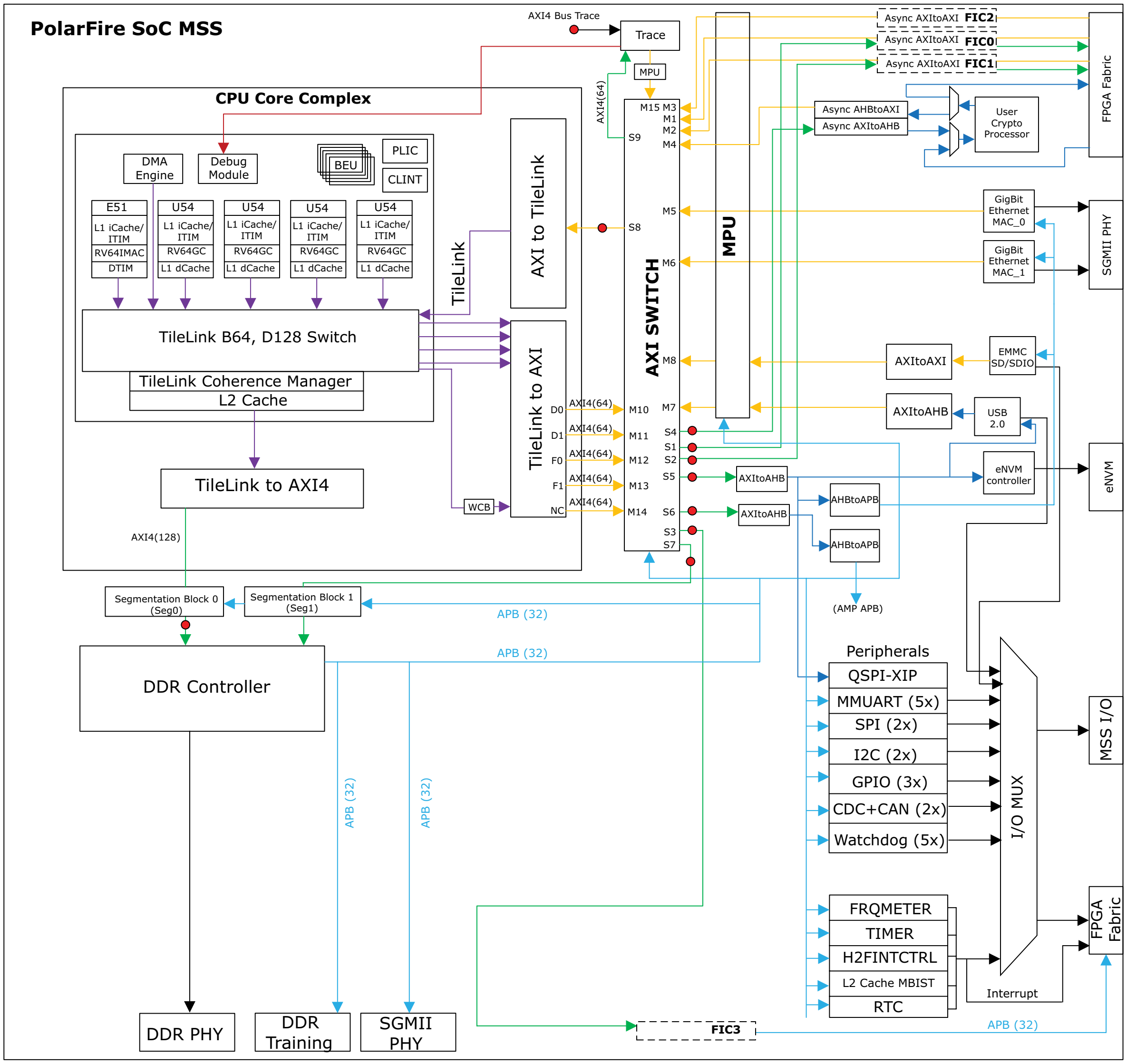
Table 8 JTAG Pin Names and Descriptions

Net Name	Pin Number	Direction	I/O Standard	Description
PF_SOC_TCK	E9	Input	3.3V	Test clock
PF_SOC_TDI	G9	Input	3.3V	Test data in
PF_SOC_TDO	E8	Output	3.3V	Test data out
PF_SOC_TMS	F8	Input	3.3V	Test mode select
PF_SOC_nTRST	G8	Input	3.3V	Test reset

6. MSS Configuration

TBD Body text

Figure 9 MSS Detailed Block Diagram



Notes:

All AXI buses with red dot are fed into the Trace Block for monitoring

The direction of arrows indicates control (master to slave).

The flow of data is bi-directional: AXI 32/64-bit, AXI 64-bit, AHB 32-bit, APB 32-bit.

Legend:

- Coherence Manager (CM) Link
- AXI Master
- AXI Slave
- AHB
- APB

6.1. eMMC Interface

The Tachyon has 8 GB of non-volatile eMMC flash memory. This device is used to store images for the RISC-V MSS. The device is connected to MSS I/Os on Bank 4.

- Part number: SDINBDG4-8G
- Manufacturer: SanDisk

Figure 10 eMMC Block Diagram

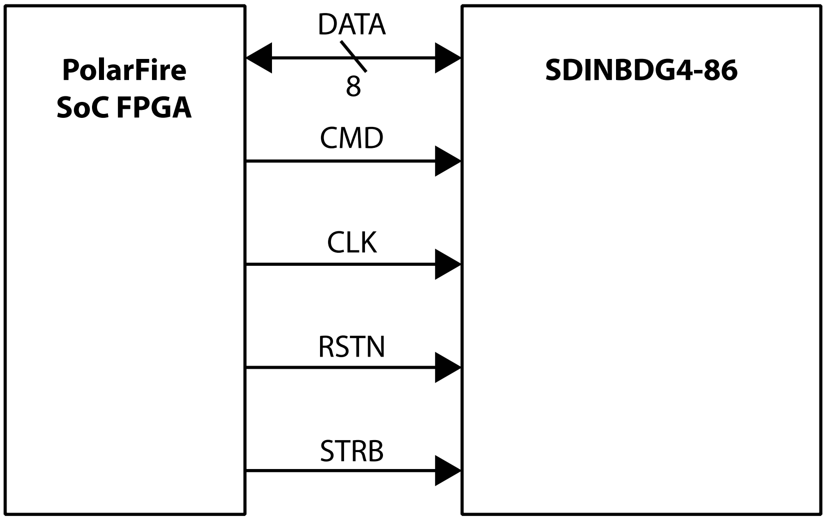


Table 9 eMMC Pin Names And Descriptions

Net Name	Pin Number	Direction	I/O Standard	Description
EM_DAT0	H1	Bidirectional	3.3V	Data bit 0
EM_DAT1	J4	Bidirectional	3.3V	Data bit 1
EM_DAT2	K4	Bidirectional	3.3V	Data bit 2
EM_DAT3	J7	Bidirectional	3.3V	Data bit 3
EM_DAT4	J6	Bidirectional	3.3V	Data bit 4
EM_DAT5	H6	Bidirectional	3.3V	Data bit 5
EM_DAT6	J3	Bidirectional	3.3V	Data bit 6
EM_DAT7	H2	Bidirectional	3.3V	Data bit 7
EM_CMD	K5	Output	3.3V	Command
EM_CLK	J1	Output	3.3V	Clock
EM_RSTN	H4	Output	3.3V	Active low reset
EM_STRB	K3	Output	3.3V	Data strobe

6.2. USB to UART Interface

The Tachyon supports four lanes of UART over USB connected to dedicated MSS I/O pins on Bank 1 of the SoC.

- Part number: CP2108-B02-GM
- Manufacturer: Silicon Labs

Figure 11 USB to UART Block Diagram

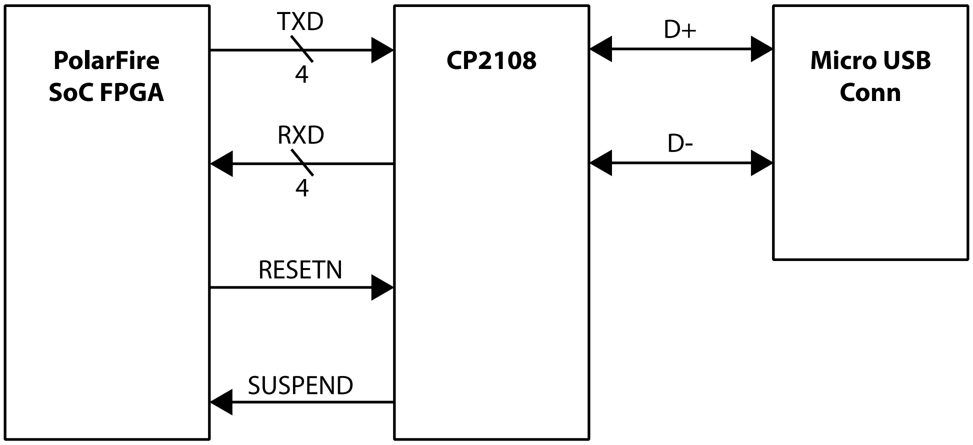


Table 10 UART Pin Names and Descriptions

Net Name	Pin Number	Direction	I/O Standard	Description
CP2108_1_RXD	F15	Input	3.3V	UART 1 RX Data
CP2108_1_TXD	B14	Output	3.3V	UART 1 TX Data
CP2108_2_RXD	G13	Input	3.3V	UART 2 RX Data
CP2108_2_TXD	E13	Output	3.3V	UART 2 TX Data
CP2108_3_RXD	C22	Input	3.3V	UART 3 RX Data
CP2108_3_TXD	B22	Output	3.3V	UART 3 TX Data
CP2108_4_RXD	B21	Input	3.3V	UART 4 RX Data
CP2108_4_TXD	D21	Output	3.3V	UART 4 TX Data
CP2108_RESETN	D22	Output	3.3V	CP2108 active low device reset
CP2108_SUS-PEND	D17	Input	3.3V	Indicates USB has entered suspend mode

6.3. I2C Interface

The MSS has two I2C interface connections avalible to external pins. The first I2C bus is used to connected to the on-board power monitor and programmable clock via Bank 2. The second I2C bus is connected from Bank 1 to the dedicated I2C pins on the VNX connector.

Figure 12 I2C Map

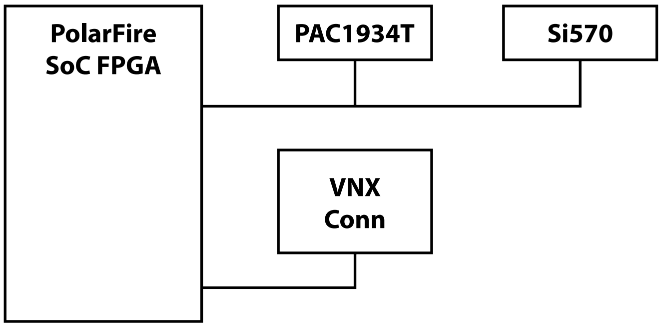


Table 11 I2C Pin Names and Descriptions

Net Name	Pin Number	Direction	I/O Standard	Description
VNX_I2C_SDA	F13	Bidirectional	3.3V	VNX I2C serial data
VNX_I2C_SCL	F12	Output	3.3V	VNX I2C serial clock
PF_I2C_SDA	B1	Bidirectional	3.3V	On-board I2C serial data
PF_I2C_SCL	C1	Output	3.3V	On-board I2C serial clock

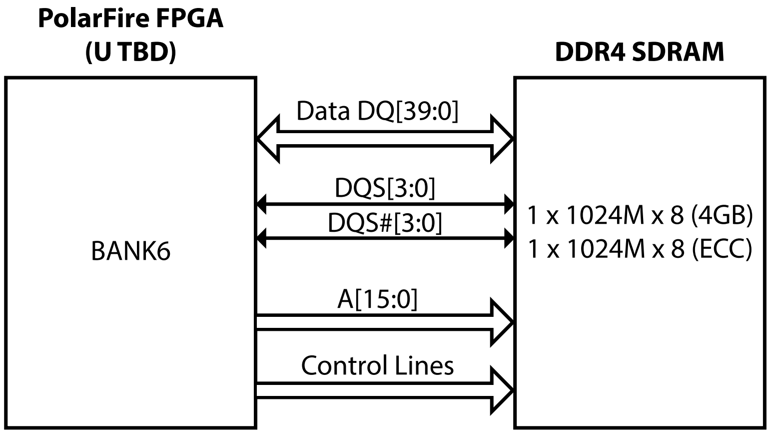
7. DDR4 Memory

The DDR memory subsystem is comprised of five 8Gb x8 DDR4 devices. This configuration offers 4 GB of ECC protected DDR4 SDRAM.

- Part Number: MT40A1G8SA (Micron)
- Supply Voltage: 1.2V, 2.5V
- Datapath width: 8 bits
- Data rate: 1600 Mb/s

The DDR subsystem is connected to the PolarFire SoC RISC-V processor subsystem's memory controller. Full functionality of the memory controller is described in UG0906: PolarFire SoC FPGA DDR Memory Controller (ref TBD).

Figure 13 DDR4 Memory



8. GPIO

8.1. LEDs

The Tachyon has four LEDs connected to the fabric via Bank 0 for debug purposes.

Figure 14 LED Interface Block Diagram

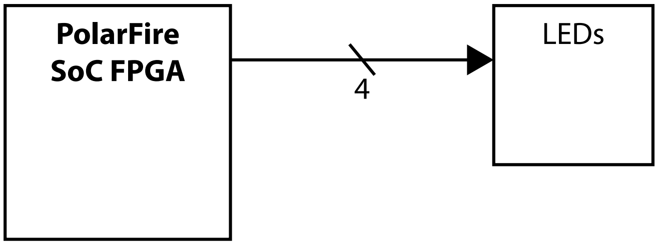


Table 12 LED Pin Names and Descriptions

Net Name	Pin Number	Direction	I/O Standard	Description
LED1	V14	Output	1.8V	LED 1
LED2	U13	Output	1.8V	LED 2
LED3	T12	Output	1.8V	LED 3
LED4	AB19	Output	1.8V	LED 4

8.2. VNX GPIO

The following pins are brought out to the VNX connector single ended and differential pair pins.

Table 13 TBD

Net Name	Pin Number	Direction	I/O Standard	Description

9. Transceivers

The PolarFire SoC has one four lane transceiver block. All four transceiver lanes are brought out the to VNX connector. The transceivers support data rates from 205 Mbps up to 12.7 Gbps. All lanes are connected to VNX S1 differential pairs as described below.

Table 14 PolarFire Transceiver Mapping

PolarFire XCVR Signal (pin number)	VNX Pin Number
XCVR_0_TX0_N (F21)	D18
XCVR_0_TX0_P (F22)	D17
XCVR_0_TX1_N (H21)	D22
XCVR_0_TX1_P (H22)	D21
XCVR_0_TX2_N (P21)	D26
XCVR_0_TX2_P (P22)	D25
XCVR_0_TX3_N (T22)	D30
XCVR_0_TX3_P (T21)	D29
XCVR_0_RX0_N (G19)	C20
XCVR_0_RX0_P (G20)	C19
XCVR_0_RX1_N (K21)	C24
XCVR_0_RX1_P (K22)	C23
XCVR_0_RX2_N (M21)	C28
XCVR_0_RX2_P (M22)	C27
XCVR_0_RX3_N (R19)	C32
XCVR_0_RX3_P (R20)	C31

Table 15 VNX Connector Row A Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
A1		GA0	Geographical Address 0
A2		GA1	Geographical Address 1
A3		GA2	Geographical Address 2
A4		UD	User-Defined -- available for general user I/O
A5		GND	Ground
A6		UD	User-Defined -- available for general user I/O
A7		UD	User-Defined -- available for general user I/O
A8		GND	Ground
A9		UD	User-Defined -- available for general user I/O
A10		UD	
A11		GND	Ground
A12		UD	
A13		GND	Ground
A14		UD	
A15		GND	Ground
A16		RFU	Reserved for future use
A17		GND	Ground
A18		GND	Ground
A19		S1_DP9_P	
A20		S1_DP9_N	
A21		GND	Ground
A22		GND	Ground
A23		S1_DP11_P	
A24		S1_DP11_N	
A25		GND	Ground
A26		GND	Ground
A27		S1_DP13_P	
A28		S1_DP13_N	
A29		GND	Ground
A30		GND	Ground
A31		S1_DP15_P	
A32		S1_DP15_N	
A33		GND	Ground
A34		S2_SE3	User-defined single-ended signals
A35		GND	Ground
A36		S2_SE7	User-defined single-ended signals
A37		GND	Ground
A38		S2_SE11	User-defined single-ended signals
A39		GND	Ground
A40		S2_SE15	User-defined single-ended signals
A41		GND	Ground
A42		S2_SE19	User-defined single-ended signals
A43		GND	Ground
A44		S2_SE23	User-defined single-ended signals
A45		GND	Ground
A46		S2_SE27	User-defined single-ended signals
A47		GND	Ground
A48		S2_SE31	User-defined single-ended signals
A49		GND	Ground
A50		S2_SE35	User-defined single-ended signals

Table 16 VNX Connector Row B Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
B1		VSBY	
B2		VSBY	
B3		GND	Ground
B4		UD	User-Defined -- available for general user I/O
B5		GND	Ground
B6		UD	User-Defined -- available for general user I/O
B7		UD	User-Defined -- available for general user I/O
B8		GND	Ground
B9		SYSRESET*	System Reset
B10		GND	Ground
B11		UD	User-Defined -- available for general user I/O
B12		GND	Ground
B13		UD	User-Defined -- available for general user I/O
B14		GND	Ground
B15		UD	User-Defined -- available for general user I/O
B16		GND	Ground
B17		S1_DP8_P	
B18		S1_DP8_N	
B19		GND	Ground
B20		GND	Ground
B21		S1_DP10_P	
B22		S1_DP10_N	
B23		GND	Ground
B24		GND	Ground
B25		S1_DP12_P	
B26		S1_DP12_N	
B27		GND	Ground
B28		GND	Ground
B29		S1_DP14_P	
B30		S1_DP14_N	
B31		GND	Ground
B32		GND	Ground
B33		S2_SE1	User defined single ended signals.
B34		GND	Ground
B35		S2_SE5	User defined single ended signals.
B36		GND	Ground
B37		S2_SE9	User defined single ended signals.
B38		GND	Ground
B39		S2_SE13	User defined single ended signals.
B40		GND	Ground
B41		S2_SE17	User defined single ended signals.
B42		GND	Ground
B43		S2_SE21	User defined single ended signals.
B44		GND	Ground
B45		S2_SE25	User defined single ended signals.
B46		GND	Ground
B47		S2_SE29	User defined single ended signals.
B48		GND	Ground
B49		S2_SE33	User defined single ended signals.
B50		GND	Ground

Table 17 VNX Connector Row C Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
C1		GND	Ground
C2		GND	Ground
C3		GND	Ground
C4		GND	Ground
C5		GND	Ground
C6		GND	Ground
C7		GND	Ground
C8		I2CDATA	I2C System Management Bus
C9		GND	Ground
C10		UD	User-Defined -- available for general user I/O
C11		GND	Ground
C12		UD	User-Defined -- available for general user I/O
C13		GND	Ground
C14		GND	Ground
C15		UD	User-Defined -- available for general user I/O
C16		UD	User-Defined -- available for general user I/O
C17		GND	Ground
C18		GND	Ground
C19		S1_DP1_P	
C20		S1_DP1_N	
C21		GND	Ground
C22		GND	Ground
C23		S1_DP3_P	
C24		S1_DP3_N	
C25		GND	Ground
C26		GND	Ground
C27		S1_DP5_P	
C28		S1_DP5_N	
C29		GND	Ground
C30		GND	Ground
C31		S1_DP7_P	
C32		S1_DP7_N	
C33		GND	Ground
C34		S2_SE2	User defined single ended signals
C35		GND	Ground
C36		S2_SE6	User defined single ended signals
C37		GND	Ground
C38		S2_SE10	User defined single ended signals
C39		GND	Ground
C40		S2_SE14	User defined single ended signals
C41		GND	Ground
C42		S2_SE18	User defined single ended signals
C43		GND	Ground
C44		S2_SE22	User defined single ended signals
C45		GND	Ground
C46		S2_SE26	User defined single ended signals
C47		GND	Ground
C48		S2_SE30	User defined single ended signals
C49		GND	Ground
C50		S2_SE34	User defined single ended signals

Table 18 VNX Connector Row D Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
D1		GND	Ground
D2		GND	Ground
D3		GND	Ground
D4		GND	Ground
D5		GND	Ground
D6		GND	Ground
D7		GND	Ground
D8		I2CCLK	I2C System Management Bus
D9		GND	Ground
D10		UD	User defined - available for general user I/O
D11		GND	Ground
D12		GND	Ground
D13		CLK3_P	PCI Express Clocks 100 MHz
D14		CLK3_N	PCI Express Clocks 100 MHz
D15		GND	Ground
D16		GND	Ground
D17		S1_DP0_P	Differential pair 0
D18		S1_DP0_N	Differential pair 0
D19		GND	Ground
D20		GND	Ground
D21		S1_DP2_P	Differential pair 2
D22		S1_DP2_N	Differential pair 2
D23		GND	Ground
D24		GND	Ground
D25		S1_DP4_P	Differential pair 4
D26		S1_DP4_N	Differential pair 4
D27		GND	Ground
D28		GND	Ground
D29		S1_DP6_P	Differential pair 6
D30		S1_DP6_N	Differential pair 6
D31		GND	Ground
D32		GND	Ground
D33		S2_SE0	User defined single ended signals
D34		GND	Ground
D35		S2_SE4	User defined single ended signals
D36		GND	Ground
D37		S2_SE8	User defined single ended signals
D38		GND	Ground
D39		S2_SE12	User defined single ended signals
D40		GND	Ground
D41		S2_SE16	User defined single ended signals
D42		GND	Ground
D43		S2_SE20	User defined single ended signals
D44		GND	Ground
D45		S2_SE24	User defined single ended signals
D46		GND	Ground
D47		S2_SE28	User defined single ended signals
D48		GND	Ground
D49		S2_SE32	User defined single ended signals
D50		GND	Ground

Table 19 VNX Connector Row E Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
E1		VS1	
E2		VS1	
E3		VS2	
E4		VS2	
E5		VS3	
E6		VBAT	
E7		GND	Ground
E8		NVMRO	
E9		UD	User Defined - available for general user I/O
E10		GND	Ground
E11		RFU	Reserved for future use
E12		RFU	Reserved for future use
E13		GND	Ground
E14		GND	Ground
E15		CLK2_P	PCI Express clock 2 - 100MHz
E16		CLK2_N	PCI Express clock 2 - 100MHz
E17		GND	Ground
E18		GND	Ground
E19		PCIE_L4_RX_P	
E20		PCIE_L4_RX_N	
E21		GND	Ground
E22		GND	Ground
E23		PCIE_L5_RX_P	
E24		PCIE_L5_RX_N	
E25		GND	Ground
E26		GND	Ground
E27		PCIE_L6_RX_P	
E28		PCIE_L6_RX_N	
E29		GND	Ground
E30		GND	Ground
E31		PCIE_L7_RX_P	
E32		PCIE_L7_RX_N	
E33		GND	Ground
E34		GND	Ground
E35		S2_DP3_P	
E36		S2_DP3_N	
E37		GND	Ground
E38		GND	Ground
E39		S2_DP7_P	
E40		S2_DP7_N	
E41		GND	Ground
E42		GND	Ground
E43		S2_DP11_P	
E44		S2_DP11_N	
E45		GND	Ground
E46		GND	Ground
E47		S2_DP15_P	
E48		S2_DP15_N	
E49		GND	Ground
E50		GND	Ground

Table 20 VNX Connector Row F Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
F1		VS1	12V Supply
F2		VS1	12V Supply
F3		VS2	5V Supply
F4		VS2	5V Supply
F5		VS3	3.3V Supply
F6		UD	User defined - available for general user I/O
F7		GND	Ground
F8		UD	User defined - available for general user I/O
F9		GND	Ground
F10		UD	User defined - available for general user I/O
F11		GND	Ground
F12		GND	Ground
F13		CLK1_P	PCI Express clock 1 - 100MHz
F14		CLK1_N	PCI Express clock 1 - 100MHz
F15		GND	Ground
F16		GND	Ground
F17		PCIE_L4_TX_P	
F18		PCIE_L4_TX_N	
F19		GND	Ground
F20		GND	Ground
F21		PCIE_L5_TX_P	
F22		PCIE_L5_TX_N	
F23		GND	Ground
F24		GND	Ground
F25		PCIE_L6_TX_P	
F26		PCIE_L6_TX_N	
F27		GND	Ground
F28		GND	Ground
F29		PCIE_L7_TX_P	
F30		PCIE_L7_TX_N	
F31		GND	Ground
F32		GND	Ground
F33		S2_DP1_P	
F34		S2_DP1_N	
F35		GND	Ground
F36		GND	Ground
F37		S2_DP5_P	
F38		S2_DP5_N	
F39		GND	Ground
F40		GND	Ground
F41		S2_DP9_P	
F42		S2_DP9_N	
F43		GND	Ground
F44		GND	Ground
F45		S2_DP13_P	
F46		S2_DP13_N	
F47		GND	Ground
F48		GND	Ground
F49		S2_DP17_P	
F50		S2_DP17_N	

Table 21 VNX Connector Row G Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
G1		VS1	12V Supply
G2		VS1	12V Supply
G3		VS2	5V Supply
G4		VS2	5V Supply
G5		VS3	3.3V Supply
G6		VS4	-12V Supply
G7		GND	Ground
G8		RFU	Reserved for future use
G9		UD	User Defined - available for general user I/O
G10		GND	Ground
G11		RFU	Reserved for future use
G12		RFU	Reserved for future use
G13		GND	Ground
G14		GND	Ground
G15		CLK0_P	PCI Express clock 0 - 100MHz
G16		CLK0_N	PCI Express clock 0 - 100MHz
G17		GND	Ground
G18		GND	Ground
G19		PCIE_L0_RX_P	
G20		PCIE_L0_RX_N	
G21		GND	Ground
G22		GND	Ground
G23		PCIE_L1_RX_P	
G24		PCIE_L1_RX_N	
G25		GND	Ground
G26		GND	Ground
G27		PCIE_L2_RX_P	
G28		PCIE_L2_RX_N	
G29		GND	Ground
G30		GND	Ground
G31		PCIE_L3_RX_P	
G32		PCIE_L3_RX_N	
G33		GND	Ground
G34		GND	Ground
G35		S2_DP3_P	
G36		S2_DP3_N	
G37		GND	Ground
G38		GND	Ground
G39		S2_DP7_P	
G40		S2_DP7_N	
G41		GND	Ground
G42		GND	Ground
G43		S2_DP11_P	
G44		S2_DP11_N	
G45		GND	Ground
G46		GND	Ground
G47		S2_DP15_P	
G48		S2_DP15_N	
G49		GND	Ground
G50		GND	Ground

Table 22 VNX Connector Row H Signals

Pin Number	Application Signal Name	VNX Signal Name	Description
H1		VS1	12V Supply
H2		VS1	12V Supply
H3		VS2	5V Supply
H4		VS2	5V Supply
H5		VS3	3.3V Supply
H6		VS4	-12V Supply
H7		GND	Ground
H8		RFU	Reserved for future use
H9		GND	Ground
H10		UD	User Defined - available for general user I/O
H11		GND	Ground
H12		GND	Ground
H13		UD	User Defined - available for general user I/O
H14		RFU	Reserved for future use
H15		GND	Ground
H16		GND	Ground
H17		PCIE_L0_TX_P	
H18		PCIE_L0_TX_N	
H19		GND	Ground
H20		GND	Ground
H21		PCIE_L1_TX_P	
H22		PCIE_L1_TX_N	
H23		GND	Ground
H24		GND	Ground
H25		PCIE_L2_TX_P	
H26		PCIE_L2_TX_N	
H27		GND	Ground
H28		GND	Ground
H29		PCIE_L3_TX_P	
H30		PCIE_L3_TX_N	
H31		GND	Ground
H32		GND	Ground
H33		S2_DP0_P	
H34		S2_DP0_N	
H35		GND	Ground
H36		GND	Ground
H37		S2_DP4_P	
H38		S2_DP4_N	
H39		GND	Ground
H40		GND	Ground
H41		S2_DP8_P	
H42		S2_DP8_N	
H43		GND	Ground
H44		GND	Ground
H45		S2_DP12_P	
H46		S2_DP12_N	
H47		GND	Ground
H48		GND	Ground
H49		S2_DP18_P	
H50		S2_DP18_N	

10. References

- ANSI/VITA 74.0-2017: Compliant System Small Form Factor Module Base Standard, ANSI/VITA, 2017
- DS0141: PolarFire Datasheet, Revision 1.7, Microsemi, 2019
- UG0676: PolarFire FPGA Memory Controller User Guide, Revision 5.0, Microsemi, 2019
- UG0677: PolarFire FPGA Transceiver User Guide, Revision 5.0, Microsemi, 2019

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