Final Project Report

March.9, 2021

1. Introduction

This report will be organized in the following three sections:

- Structure - The models in the Spice netlist will be first described, including a decoder, a write block, a read block, a memory cell and a wire model.
- Function - To test the functionality of our SRAM model, we will run simulation in HSPICE. Memory cells 0, 96, 144, and 255 will be written and then read. By examining obtained waveforms, we can check the correctness of our simulated netlist.
- Performance - We will evaluate the performance of our SRAM design by measuring the transition time and shortest clock period.

2. Structure

I. Decoder model

The full 8bit decoder can be realized with 2 4bit decoders and 16 groups of 16 NAND/AND gates. For simulation simplification, we just need to simulate a single 4bit decoder to enable a single memory cell (or a single word).

The structure of our 4bit decoder model is shown in Fig. 1. It is composed of 6 stages. When the input signal ad0 is LO and the clock signal clk is HI, the output signal ope is asserted and set to LO for the memory cell to be operated. The fanout pins for other cells are floating.

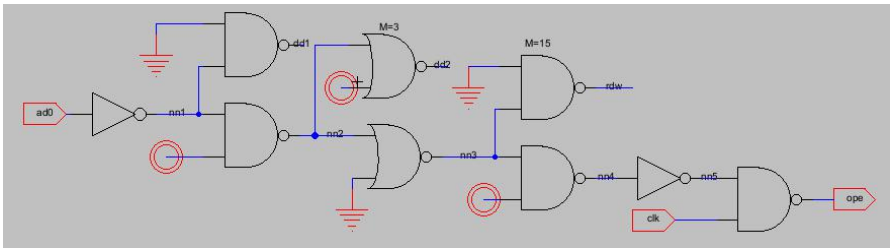

Fig. 1. Decoder model.

II. Write block model

The write block model consists of 2 pmos transistors, 3 nmos transistors, 2 inverters and 1 NAND gate, as shown in Fig. 2. When the clock signal clk is HI and operation control signal rwt is LO, a write operation is carried out. The data to be written into the memory cell depends on the data input signal dii. If dii is HI, the left bitline btt is pulled down to GND, which further leads to the state flip of the memory cell. Similarly, if dii is LO, the right bitline is pulled down to GND, causing the state of the memory cell to flip to the opposite.

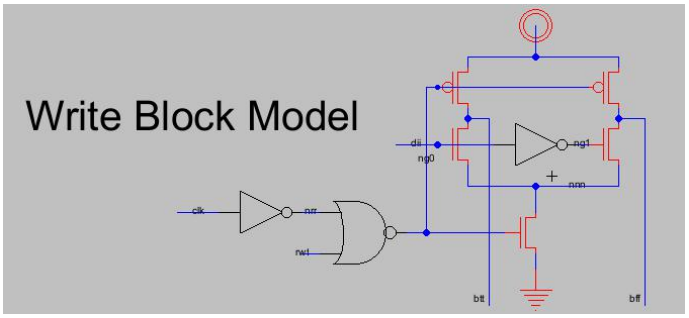

Fig. 2. Write block model.

III. Read block model

The read block model can be further divided into two parts, namely readSub and readCollect,

which are shown in Fig. 3 and Fig.4, respectively. The readSub model takes the clock signal clk, the operation control signal rwt and address flag add as input. If clk is HI, rwt is HI and address matches (add = HI), voltage on the two bitlines will be sensed by the sense amplifier. Then, readCollect model takes the outputs of the 8 sense amplifiers, and then choose the right one to output at doi by making one of the eight transistors transparent.

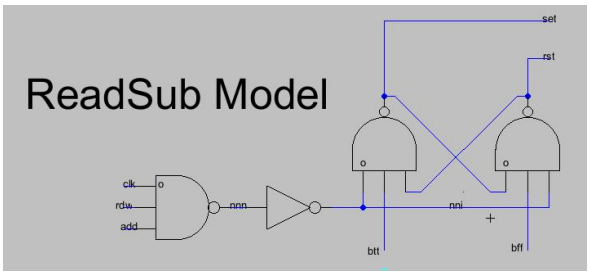

Fig. 3. ReadSub model.

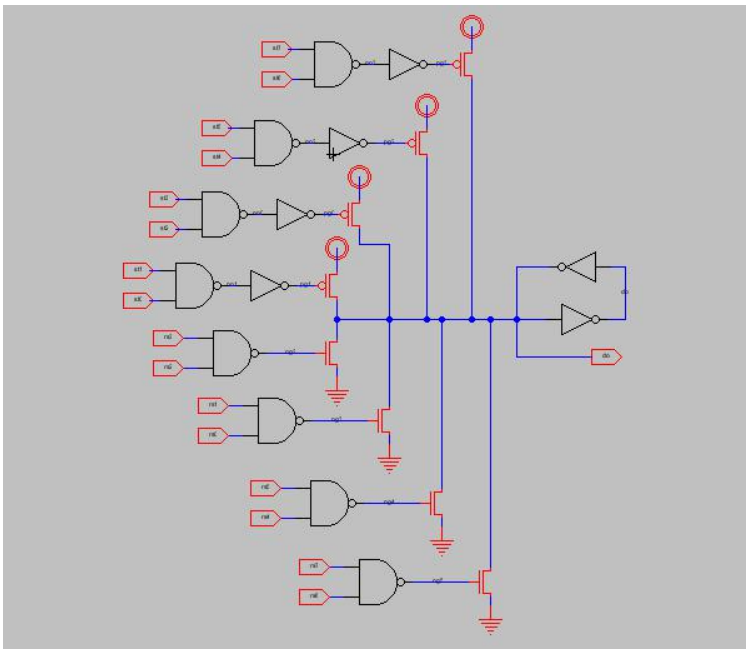

Fig. 4. ReadCollect model.

IV. Memory cell model

The SRAM memory cell consists of 6 transistors, as shown in Fig. 5.

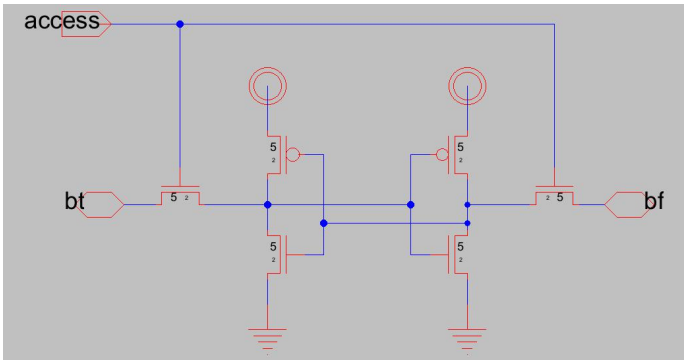

Fig. 5. Memory cell model.

To write the memory cell, access input should be set to HI to turn on the access transistors. By pulling down the voltage to GND on the left bitline or the right bitline, the voltage of the internal

nodes will be changed. To read the memory cell, access input should be set to HI. The different voltages on the internal nodes will then cause a voltage different on the two bitlines.

The layout of the SRAM memory cell is plotted in Fig. 6. Each cell has a height of 33λ and width of 66λ (overlapping in the memory cell array considered).

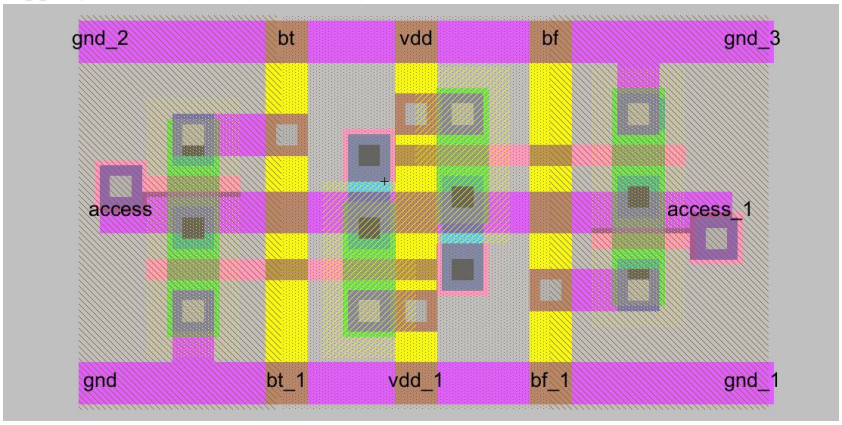

Fig. 6. Memory cell layout.

V. Wire model

In our design, an SRAM with a capacity of 256 8bit words is divided into eight subarrays, each of which has 32 words and connects to a write block and a read block separately. Thus, the length of the subarray bitlines is 32 times the height of a single memory cell, which is 1056λ. Besides, the width of the bitlines is 4λ.

3. Function

I. Write function

The write function is verified with HSPICE file “testMem.cir”. We will write data to different locations in the cell array, namely bit 0, 96, 144 and 255.

The control and input signals for writing the four bits are shown in Figure 7. The top trace is the clock signal clk. To test the functionality, we did not choose a extremely short clock period. Instead, it is selected as 20 ns. The second trace is the address flag ad0. When ad0 is LO, the corresponding memory cell is selected. The third trace is the data input dii. The last trace is the signal to control the access transistors of the memory cell. It is generated from the clk and ad0. It can be inferred that 1 should be written at 20ns, and 0 should be written at 40ns.

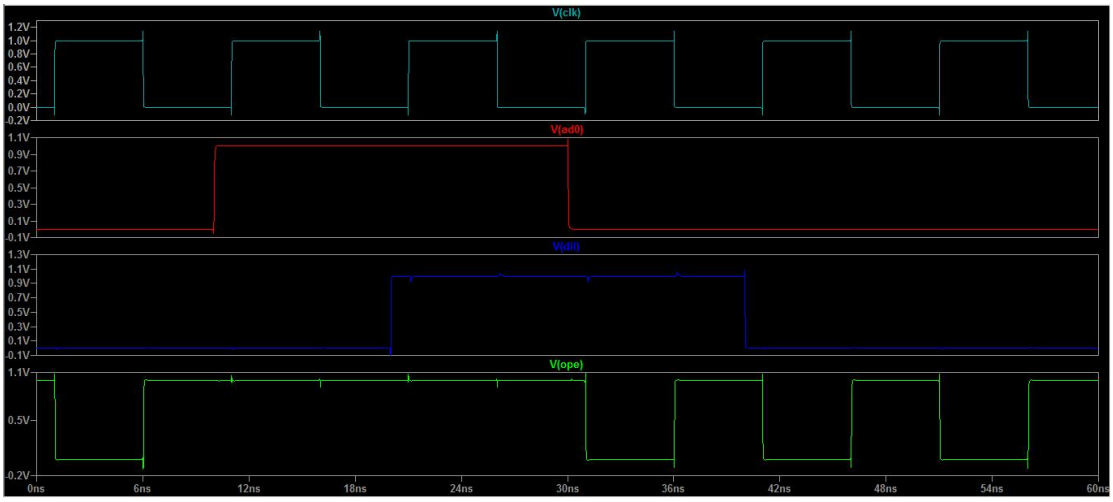

Fig. 7. Waveforms of clock, address flag, data input and access signals.

The waveform of writing bit 0 is shown in Fig. 8. It is noted that the transitions should be the fastest since bit 0 cell is right next to the write block.

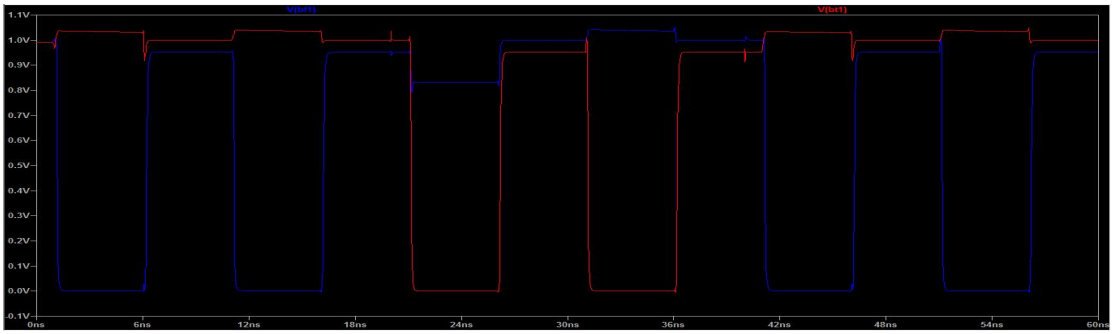

Fig. 8. Waveforms of bitlines beside bit 0 cell.

Similarly, we wrote 1 and 0 into bit 96, 144 and 255, waveforms of which are shown in Fig. 9-11, respectively. Since the 256 word SRAM is divided into 4 subarrays, bit 96 is located in the 32nd position of the second subarray, bit 144 is located in the 16th position of the third subarray, and bit 255 is located at the bottom of the fourth subarray, right next to the read block. It is observed that the farther the cell away from the write block, the slower rising or falling transitions.

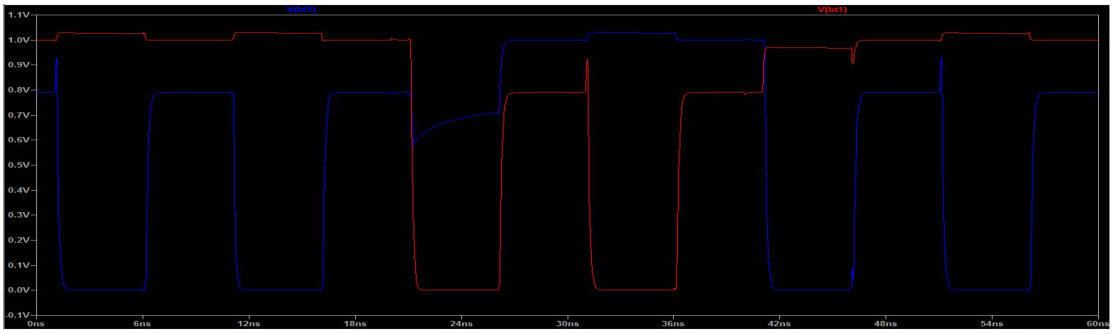

Fig. 9. Waveforms of bitlines beside bit 96 cell.

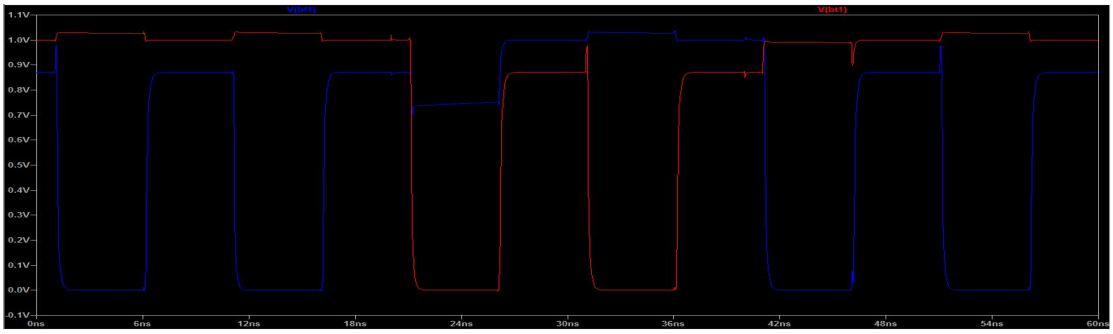

Fig. 10. Waveforms of bitlines beside bit 144 cell.

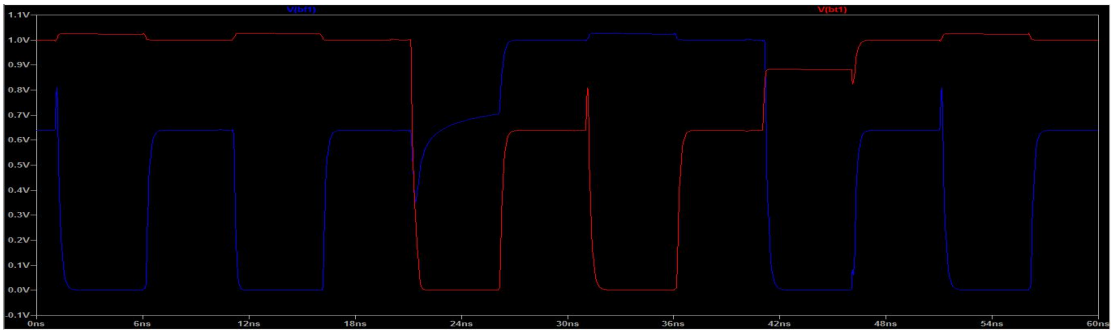

Fig. 11. Waveforms of bitlines beside bit 255 cell.

II. Read function

The read function is verified with HSPICE file “testBuffer.cir”. We will read data from different locations in the cell array, namely bit 0, 96, 144 and 255.

The control and input signals for reading the four bits are shown in Figure 12. The top trace is the clock signal clk. To test the functionality, we did not choose a extremely short clock period. Instead, it is selected as 20 ns. The second trace is the operation control signal rdw. When rdw is HI, the read operation will be carried out. When rdw is LO, the write operation will be carried out. The last trace is the data input dii. It can be inferred that data 0 should be written into the cell at 60ns, then it is read out at 80ns. Besides, data 1 should be written into the cell at 100ns and read out at 120ns.

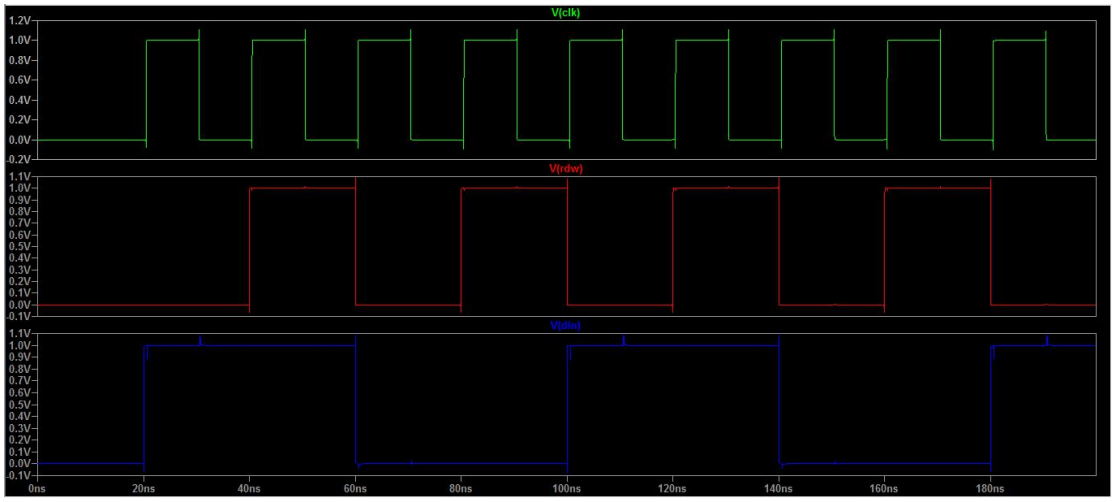

Fig. 12. Waveforms of clock, operation control and data input signals.

The resulting waveforms of bit 0, 96, 144 and 255 are shown in Fig. 13-16, respectively. The read and writing operations for the four cells are carried out correctly. However, it can be found that the farther the cell away from the read block, the smaller voltage difference between the two bitlines, which means that the read operations become more and more difficult because the sense margin for the sense amplifier is decreasing.

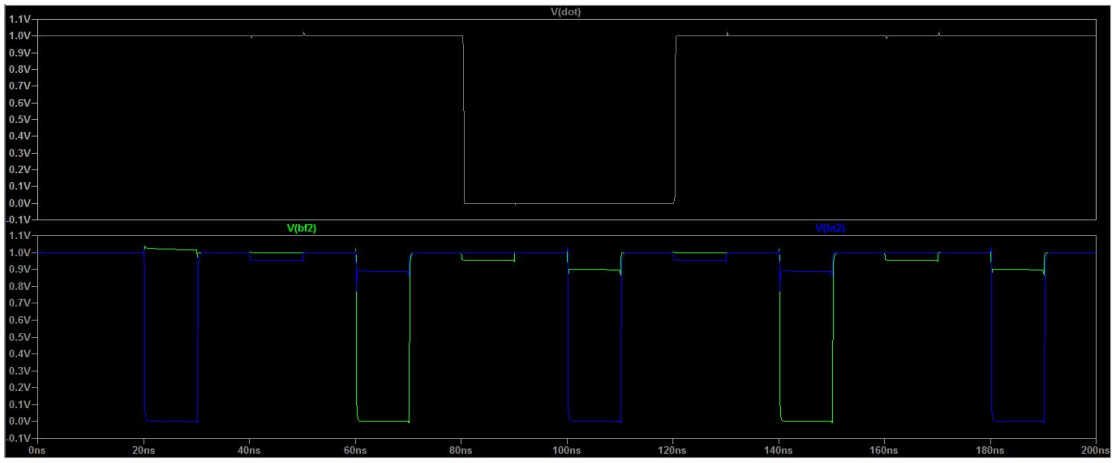

Fig. 13. Waveforms of bitlines beside bit 0 cell.

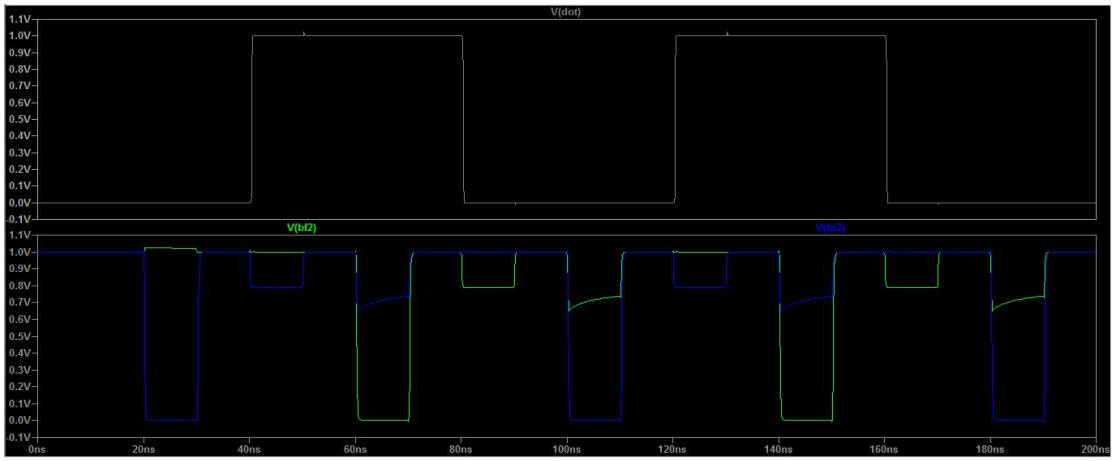

Fig. 14. Waveforms of bitlines beside bit 96 cell.

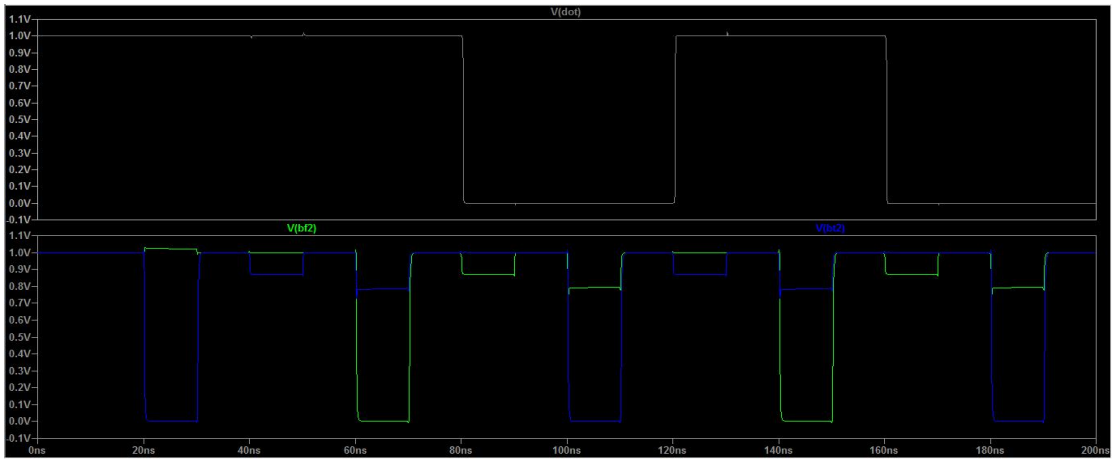

Fig. 15. Waveforms of bitlines beside bit 144 cell.

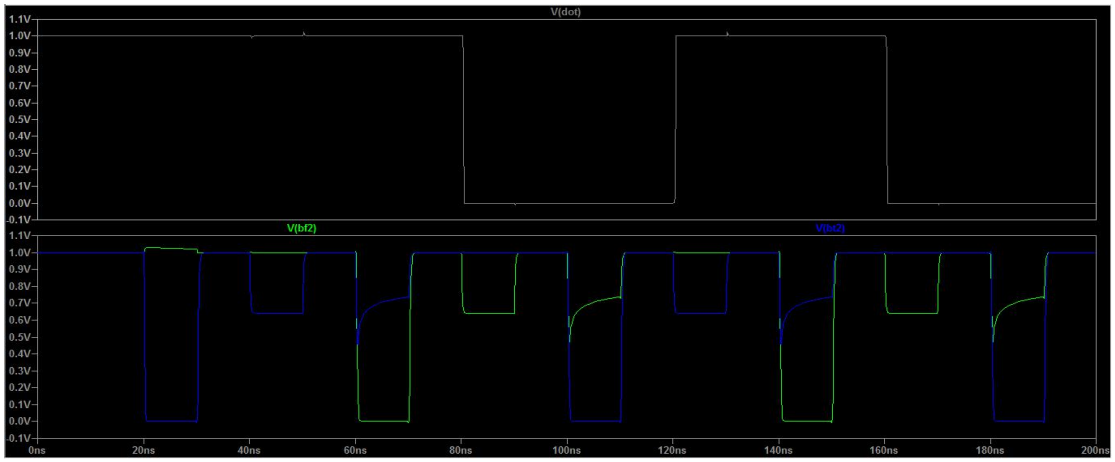

Fig. 16. Waveforms of bitlines beside bit 255 cell.

4. Performance

We evaluate the performance by looking for the shortest clock period that allows our SRAM to work correctly. The shortest period we measured is 3.5ns.